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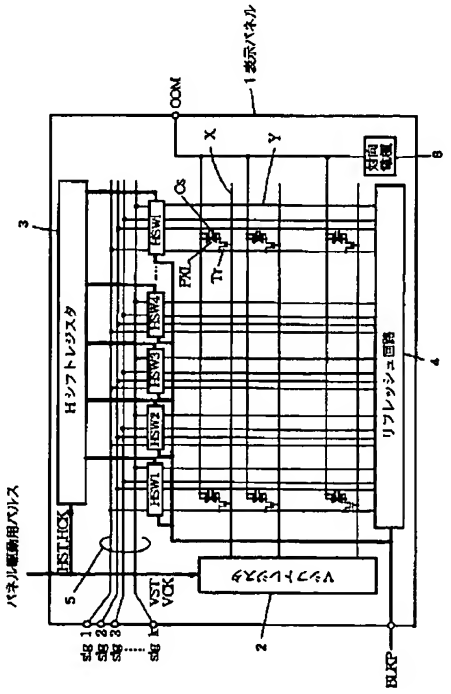
(54)【発明の名称】　アクティブマトリクス表示装置

(57)【要約】
【課題】　アクティブマトリクス表示装置をパネルに用いたディスプレイシステムの全体としての消費電力を抑制する。
【解決手段】　アクティブマトリクス表示装置１は行状のゲート線Ｘと、列状の信号線Ｙと、両者の交差部に配された行列状の画素ＰＸＬと、各ゲート線Ｘを線順次走査し一水平期間毎に一行分の画素ＰＸＬを選択するＶシフトレジスタ２と、一水平期間内で外部から供給された映像信号ｓｉｇ１～ｓｉｇｋを各信号線Ｙにサンプリングし選択された一行分の画素ＰＸＬに映像信号ｓｉｇ１～ｓｉｇｋの書き込みを行なうＨシフトレジスタ３とを有する。更に、リフレッシュ回路４を備えており、映像信号ｓｉｇ１～ｓｉｇｋのブランキング期間に信号線Ｙを外部から一時的に切り離すとともに、互いに反対極性の映像信号ｓｉｇ１～ｓｉｇｋがサンプリングされていた複数の信号線Ｙをブランキング期間で内部的に短絡させ、各信号線Ｙの電荷を外部から切り離した状態で内部的に中和する。



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【特許請求の範囲】

【請求項１】　行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部から供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号の書き込みを行なう水平駆動回路とを有するアクティブマトリクス表示装置であって、

映像信号のブランキング期間に信号線を外部から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ各信号線の電荷を外部から切り離した状態で内部的に中和するリフレッシュ回路を有することを特徴とするアクティブマトリクス表示装置。

【請求項２】　前記リフレッシュ回路は、全信号線を外部から切り離すとともに全信号線を内部的に短絡させることを特徴とする請求項１記載のアクティブマトリクス表示装置。

【請求項３】　前記リフレッシュ回路は、全信号線を複数本づつ組に分け組同志で短絡させることを特徴とする請求項１記載のアクティブマトリクス表示装置。

【請求項４】　前記水平駆動回路は、列状に配列した信号線に対して交互に反対極性の映像信号をサンプリングすることを特徴とする請求項１記載のアクティブマトリクス表示装置。

【請求項５】　所定の基準電圧に対して極性が反転する映像信号を供給するビデオドライバと、該映像信号に同期して制御信号を供給するタイミングジェネレータと、該制御信号に応じて動作し該映像信号に基づいて映像を表示する表示パネルとからなるディスプレイシステムであって、

前記表示パネルは、行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部の該ビデオドライバから供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号を書き込んで映像を表示する水平駆動回路とを備え、

該タイミングジェネレータから供給された制御信号に応じて映像信号のブランキング期間に信号線を外部の該ビデオドライバから一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ各信号線の電荷を外部から切り離した状態で内部的に中和するリフレッシュ回路を有することを特徴とするディスプレイシステム。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は画面を構成する画素とこれを駆動する薄膜トランジスタなどのスイッチング素子と周辺の駆動回路とを内蔵したアクティブマトリクス表示装置（以下、表示パネルと略称する場合がある）に関する。又、所定の基準電圧に対して極性を反転する映像信号を供給するビデオドライバと、映像信号に同期して制御信号を供給するタイミングジェネレータと、制御信号に応じて動作し映像信号に基づいて映像を表示する表示パネルとからなるディスプレイシステムに関する。

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【０００２】

【従来の技術】図１５を参照して従来のアクティブマトリクス表示装置を簡単に説明する。図示する様に、表示パネル１は行状のゲート線Ｘと、列状の信号線Ｙとを備えており、両者の交差部に画素ＰＸＬが設けられている。画素ＰＸＬは一方の基板に形成された画素電極と、他方の基板に形成された対向電極６と、両者の間に保持された液晶などの電気光学物質とからなる。各画素ＰＸＬは対応する薄膜トランジスタＴｒによりスイッチング駆動される。又、各画素ＰＸＬに対応して補助容量Ｃｓも形成されている。薄膜トランジスタＴｒのゲート電極は対応するゲート線Ｘに接続され、ソース電極は対応する信号線Ｙに接続され、ドレイン電極は対応する画素電極に接続されている。表示パネル１はｋ本の入力線５を備えており、外部のビデオドライバから供給されるｋ個の映像信号ｓｉｇ１，ｓｉｇ２，・・・，ｓｉｇｋをそれぞれ受け入れる。個々の信号線Ｙはｋ本を一単位として水平スイッチＨＳＷを介して所定の入力線５に接続されている。以上の構成に加え、表示パネル１はＶシフトレジスタ２とＨシフトレジスタ３を内蔵している。Ｖシフトレジスタ２は垂直駆動回路を構成し、外部のタイミングジェネレータから供給される垂直スタートパルスＶＳＴや垂直クロックパルスＶＣＫなどのパネル駆動用パルスに応答して動作し、ゲート線Ｘを一本づつ順次走査して画素を行毎に選択する。一方、Ｈシフトレジスタ３は同じくタイミングジェネレータから供給される水平スタートパルスＨＳＴや水平クロックパルスＨＣＫなどのパネル駆動用パルスに応答して動作し、順次サンプリングパルスを出力し対応する水平スイッチＨＳＷ１，ＨＳＷ２，・・・，ＨＳＷｉを開閉制御して、ｋ本の信号線Ｙを一単位としてまとめ駆動する。即ち、ｋ系統の映像信号ｓｉｇ１，・・・，ｓｉｇｋをそれぞれ対応する信号線Ｙに一斉サンプリングする。

【０００３】係る複数画素同時サンプリング駆動を行なう際、ｋ系統の映像信号ｓｉｇ１～ｓｉｇｋにあらかじめ画素ピッチに対応する遅延量を相対的に与える為、サンプルホールド回路がビデオドライバに設けられている。ｋ系統の映像信号を逐次サンプルホールドして画素ピッチに対応する遅延量を相対的に与えるとともに、水平スイッチＨＳＷをｋ本の信号線の組を単位として同時に開閉制御することにより、この水平スイッチを駆動するＨシフトレジスタ３に含まれる段数を削減して構成を

簡単にすることができる。なお、ＨＳＷ１～ＨＳＷｉとＨシフトレジスタ３とで水平駆動回路を構成する。

【０００４】図１６は、従来のディスプレイシステムの全体構成を示すブロック図である。ディスプレイシステムはビデオドライバ８と、図１５に示した表示パネル１と、タイミングジェネレータ（ＴＧ）９とを備えている。なお、表示パネル１は電気光学物質として液晶（ＬＣ）を用いる場合が多いので、ここではＬＣＤと呼ぶ場合がある。ビデオドライバ８は外部入力されるビデオ信号ＳＩＧを処理してＬＣＤ１の駆動に適した映像信号ｓｉｇに変換する。例えば、ビデオドライバ８は一水平期間（１Ｈ）で映像信号ｓｉｇの極性反転処理を行ない、交流化された映像信号ｓｉｇをＬＣＤ１に出力する。ＬＣＤ１は図１５に示した通り、行状のゲート線、列状の信号線、及び両者の交差部に設けた液晶画素を備えている。又、垂直駆動回路及び水平駆動回路を内蔵している。垂直駆動回路はゲート線を順次走査して画素を選択する。水平駆動回路は１Ｈ毎に交流化映像信号ｓｉｇを信号線に順次サンプリングし、選択された画素に交流化映像信号ｓｉｇを書き込む。タイミングジェネレータ９は同期信号ＳＩＮＣに応じて動作し、ビデオドライバ８に対し交流化信号ＦＲＰを供給して極性反転処理のタイミング制御を行なう。又、ビデオドライバ８に対しサンプルホールド信号ＳＨＰを供給し、映像信号ｓｉｇの遅延処理を制御している。即ち、ビデオドライバ８は画素の配列ピッチに応じ複数系統の映像信号ｓｉｇを相対的に遅延処理してＬＣＤ１に供給している。タイミングジェネレータ９は更に、ＨＳＴ，ＨＣＫ，ＶＳＴ，ＶＣＫなどのパネル駆動用パルスをＬＣＤ１に供給し、垂直駆動回路及び水平駆動回路の動作制御を行なう。

【０００５】ビデオドライバ８は、例えばクランプ回路ＣＬＰ、ブライト回路ＢＲＴ、ガンマ補正回路γ、ゲイン回路ＧＡＩＮ、反転回路ＩＮＶ．ＡＭＰ、極性反転スイッチＳＷ、サンプルホールド回路Ｓ／Ｈ、負荷駆動用バッファＢＵＦＦなどで構成されている。

【０００６】図１７を参照して、図１６に示したディスプレイシステムの動作を簡潔に説明する。外部から入力されたビデオ信号ＳＩＧはクランプ回路ＣＬＰでペデスタルクランプされ、基準となる電圧が決められる。ペデスタルクランプされた信号は、ブライト回路ＢＲＴで輝度を調整する為にブライトコントロールされる。ブライトコントロールされた信号はガンマ補正回路γでＬＣＤ１の特性に合わせたγ補正を行なう。γ補正された信号はゲイン回路ＧＡＩＮでゲイン調整を施される。ゲイン調整された信号ＡＭＰＩＮは極性反転スイッチＳＷによって交流化される。この極性反転スイッチＳＷはタイミングジェネレータ９から供給されるＦＲＰによりオン／オフ制御される。交流化された信号は複数画素同時駆動を採用するＬＣＤ１に適した位相差を付ける為、サンプルホールド回路Ｓ／Ｈを通る。なお、このサンプルホールド回路Ｓ／Ｈはタイミングジェネレータ９から供給されるＳＨＰにより制御されている。サンプルホールドされた映像信号ｓｉｇはバッファＢＵＦＦを介してＬＣＤ１に供給される。前述した様に、複数系統の映像信号ｓｉｇ１～ｓｉｇｋは順次開閉制御されるＨＳＷ１～ＳＨＷｉによってｋドット毎同時に画素に書き込まれる。なお、図１７から明らかな様に、ＬＣＤ１に供給される映像信号ｓｉｇは１Ｈ毎に所定の基準電圧に対して極性が反転している。この基準電圧は図１５に示した対向電極６に印加される共通電圧ＣＯＭにほぼ等しい。

【０００７】図１８は、ＬＣＤ１の各画素ＰＸＬに書き込まれる映像信号ｓｉｇの極性を模式的に表わしている。この例では、ｋ＝６として、６画素毎同時に６系統の映像信号ｓｉｇ１～ｓｉｇ６が書き込まれる。なお、画素ＰＸＬは全体としてｎ行ｍ列のマトリクスを構成している。本例は、所謂ドット反転駆動を採用している。ゲート線Ｘ１に対応する１ライン目では、信号線Ｙ１～Ｙ６を介して６個の画素１－１，１－２，１－３，１－４，１－５，１－６に＋－＋－＋－の極性の映像信号ｓｉｇ１～ｓｉｇ６が書き込まれる。次の２ライン目では、画素２－１，２－２，２－３，２－４，２－５，２－６に、－＋－＋－＋の極性の映像信号ｓｉｇ１～ｓｉｇ６が書き込まれる。この様に、ドット反転駆動では、ｎ×ｍの画素ＰＸＬに対して互いに反対極性の映像信号ｓｉｇが千鳥状に書き込まれる。

【０００８】

【発明が解決しようとする課題】以上の様に、通常ＬＣＤ１は液晶の劣化を防ぐ為交流駆動が必要であり、映像信号ｓｉｇを共通電圧ＣＯＭに対して反転する必要がある。この為、例えば共通電圧ＣＯＭに対して最大Ｖｍａｘの電圧を画素ＰＸＬに書き込む場合には、極性反転毎に最大で２Ｖｍａｘの電圧を遷移させる必要がある。従って、短時間の間に最大で２Ｖｍａｘの電圧を遷移させることができる能力を備えたバッファＢＵＦＦが外部のビデオドライバ８に必要となる。従来のＬＣＤを用いたディスプレイシステムでは、このバッファＢＵＦＦ及び画素ＰＸＬや信号線Ｙなどの負荷を充放電する為に大量の電流が流れており、これがディスプレイシステムの消費電力の大半を占めていた。

【０００９】この問題を解決する為、充放電の対象となる画素や信号線の負荷を軽減したり、画素に印加する電圧を低減化していた。しかしながら、前者の場合には物理的な限界があり、必ずしも充分な対策とはならない。又、後者の場合はコントラストの低下など画質劣化の副作用が現われていた。

【００１０】

【課題を解決する為の手段】上述した従来の技術の課題を解決する為に以下の手段を講じた。即ち、本発明に係るアクティブマトリクス表示装置（表示パネル）は、基本的な構成として、行状のゲート線と、列状の信号線

と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部から供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号の書き込みを行なう水平駆動回路とを有する。特徴事項として、本アクティブマトリクス表示装置はリフレッシュ回路を備えており、映像信号のブランキング期間に信号線を外部から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。好ましくは、前記リフレッシュ回路は、全信号線を外部から切り離すとともに、全信号線を内部的に短絡させる。あるいは、前記リフレッシュ回路は、全信号線を複数本づつ組に分け組同志で短絡させてもよい。なお、前記水平駆動回路は、例えば列状に配列した信号線に対して交互に反対極性の映像信号をサンプリングする。

【００１１】本発明は、上述したアクティブマトリクス表示装置を表示パネルに用いたディスプレイシステムを包含している。本ディスプレイシステムは基本的な構成として、所定の基準電圧に対して極性が反転する映像信号を供給するビデオドライバと、該映像信号に同期して制御信号を供給するタイミングジェネレータと、該制御信号に応じて動作し該映像信号に基づいて映像を表示する表示パネルとからなる。前記表示パネルは、行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部の該ビデオドライバから供給された映像信号を各信号線にサンプリングし選択された一行分の画素に映像信号を書き込んで映像を表示する水平駆動回路とを備えている。特徴事項として、本表示パネルはリフレッシュ回路を内蔵しており、該タイミングジェネレータから供給された制御信号に応じて映像信号のブランキング期間に信号線を外部の該ビデオドライバから一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線を該ブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。

【００１２】通常、ＬＣＤなどの表示パネルは映像信号を基準電圧に対して反転する為、画素に書き込む電圧の２倍を充放電する必要がある。本発明では、ブランキング期間にＬＣＤ内部で正極性の映像信号がサンプリングされた信号線と負極性の映像信号がサンプリングされた信号線を互いに短絡（ショート）し、電荷を中和（キャンセル）している。これにより、有効期間に充放電する電荷を減らし、ディスプレイシステムの低消費電力化を図っている。具体的には、アクティブマトリクス表示パネルにおいて、例えばドット反転駆動を採用した場合、

一水平期間毎の映像ブランキング期間に、全信号線をショートさせることによって、パネル内の信号線を一度基準電圧付近の電圧にリフレッシュする。この時、表示パネル内の信号線と外部のビデオドライバは完全に分離することにより、パネル内部の電荷のみでリフレッシュする。あるいは、ドット反転駆動において、一水平期間毎の映像ブランキング期間に、隣り合う複数本の信号線毎にそれぞれショートさせることによって、表示パネル内の信号線を基準電圧付近の電圧にリフレッシュすることも可能である。従来の表示パネルではビデオドライバ側で基準電圧に対して負極性側から正極性側あるいは正極性側から負極性側に信号線を充放電していた。本発明によれば、パネル内部の電荷のみで信号線の電位を基準電圧付近にリフレッシュできる為、外部回路からの充放電を大幅に削減することができ、ディスプレイシステム全体での消費電力を低減化可能である。本発明によれば、負荷を削減したり画素に書き込む電圧を低減化することなしに、低消費電力化を達成することが可能である。

【００１３】

【発明の実施の形態】以下図面を参照して本発明の実施形態を詳細に説明する。図１は、本発明に係るアクティブマトリクス表示装置（表示パネル）の基本的な構成を示す回路図である。なお、図１５に示した従来のアクティブマトリクス表示装置と対応する部分には対応する参照番号を付して理解を容易にしている。本実施形態は、所謂複数画素同時駆動方式を採用している。但し、本発明はこれに限られるものではなく、画素１個毎に映像信号を書き込む点順次方式あるいは一行分の画素に一括で映像信号を書き込む線順次方式にも適用可能である。図示する様に、表示パネル１は行状のゲート線Ｘと、列状の信号線Ｙとを備えており、両者の交差部に画素ＰＸＬが設けられている。各画素ＰＸＬは対応する薄膜トランジスタＴｒによりスイッチング駆動される。薄膜トランジスタＴｒのゲート電極は対応するゲート線Ｘに接続され、ソース電極は対応する信号線Ｙに接続され、ドレイン電極は対応する画素電極に接続されている。各画素電極は対向電極６に対面しており、両者の間に液晶などの電気光学物質が保持されている。対向電極６には外部から共通電圧ＣＯＭが印加されている。表示パネル１はｋ本の入力線５を備えており、外部のビデオドライバから供給されるｋ個の映像信号ｓｉｇ１～ｓｉｇｋをそれぞれ受け入れる。個々の信号線Ｙはｋ本を一単位として水平スイッチＨＳＷを介して所定の入力線５に接続されている。以上の構成に加え、表示パネル１はＶシフトレジスタ２とＨシフトレジスタ３を内蔵している。Ｖシフトレジスタ２は外部のタイミングジェネレータから供給される垂直スタートパルスＶＳＴや垂直クロックパルスＶＣＫなどのパネル駆動用パルスに応答して動作し、ゲート線Ｘを一本づつ順次走査して画素を行毎に選択する。即ち、Ｖシフトレジスタ２は垂直駆動回路を構成する。

一方、Ｈシフトレジスタ３は同じくタイミングジェネレータから供給される水平スタートパルスＨＳＴや水平クロックパルスＨＣＫなどのパネル駆動用パルスに応答して動作し、順次サンプリングパルスを出力し対応する水平スイッチＨＳＷ１～ＨＳＷｉを開閉制御して、ｋ本の信号線Ｙを一単位としてまとめ駆動する。即ち、ｋ系統の映像信号ｓｉｇ１～ｓｉｇｋをそれぞれ対応する信号線Ｙに一斉サンプリングする。Ｈシフトレジスタ３とＨＳＷとで水平駆動回路を構成する。

【００１４】特徴事項として、本表示パネル１はリフレッシュ回路４を備えている。このリフレッシュ回路４は外部のタイミングジェネレータから供給される制御信号ＢＬＫＰに応じて動作し、映像信号ｓｉｇ１～ｓｉｇｋのブランキング期間に信号線Ｙを外部のビデオドライバから一時的に切り離すとともに、互いに反対極性の映像信号ｓｉｇ１～ｓｉｇｋがサンプリングされていた複数の信号線Ｙをブランキング期間で内部的に短絡させ、各信号線Ｙの電荷を外部から切り離した状態で内部的に中和する。具体的には、リフレッシュ回路４はＢＬＫＰに応じて水平スイッチＨＳＷ１～ＨＳＷｉをブランキング期間中一時的にオフ状態にするとともに、リフレッシュ回路４の本体内で各信号線Ｙを電気的に接続する。

【００１５】図２はリフレッシュ回路４の具体的な構成例を示す。（Ａ）に示した例では、全信号線Ｙを外部から切り離すとともに、ＢＬＫＰに応じて全信号線Ｙを内部的に短絡させる為のスイッチＲＳＷを備えている。一方（Ｂ）の例では、信号線Ｙを例えばｋ本づつ組に分け、２組づつ互いに短絡させている。なお、本発明はこれに限られるものではなく、基本的に正極性の映像信号がサンプリングされた信号線と負極性の映像信号がサンプリングされた信号線を、同数本づつ短絡させればよい。

【００１６】図３は、本発明に係るディスプレイシステムを示すブロック図である。なお、理解を容易にする為、図１６に示した従来のディスプレイシステムと対応する部分には対応する参照番号を付している。図示する様に、本ディスプレイシステムはビデオドライバ８とタイミングジェネレータ９と表示パネル（ＬＣＤ）１とを備えている。ビデオドライバ８は所定の基準電圧に対して極性反転する映像信号ｓｉｇを供給する。タイミングジェネレータ９は映像信号ｓｉｇに同期してパネル駆動用パルスや制御信号ＢＬＫＰを供給する。ＬＣＤ１はパネル駆動用パルスや制御信号ＢＬＫＰに応じて動作し映像信号ｓｉｇに基づいて映像を表示する。前述した様に、ＬＣＤ１は行状のゲート線と、列状の信号線と、両者の各交差部に配された行列状の画素と、各ゲート線を線順次走査し一水平期間毎に一行分の画素を選択する垂直駆動回路と、一水平期間内で外部のビデオドライバ８から供給された映像信号ｓｉｇを各信号線にサンプリングし選択された一行分の画素に映像信号を書き込んで映像を表示する水平駆動回路とを備えている。なお、垂直駆動回路はＶシフトレジスタから構成されており、水平駆動回路はＨシフトレジスタと水平スイッチＨＳＷとの組合わせで構成されている。特徴事項として、ＬＣＤ１はリフレッシュ回路を内蔵している。このリフレッシュ回路はタイミングジェネレータ９から供給される制御信号ＢＬＫＰに応じて映像信号ｓｉｇのブランキング期間に信号線を外部のビデオドライバ８から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線をブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。

【００１７】図４は、本発明に係るディスプレイシステムの実施例を示すブロック図である。本実施例は６画素同時駆動方式（ｋ＝６）を採用し且つドット反転駆動方式を採用している。ビデオドライバ８はビデオ信号ＳＩＧを処理して６系統の映像信号ｓｉｇ１～６をＬＣＤ１に供給する。ｓｉｇ１～６は交流化されており且つ位相調整が施されている。ｓｉｇ１及びｓｉｇ２には例えば赤色の映像信号が割り当てられており、ｓｉｇ３及びｓｉｇ４には緑色の映像信号が割り当てられており、ｓｉｇ５及びｓｉｇ６には青色の映像信号が割り当てられている。タイミングジェネレータ９は同期信号ＳＹＮＣに応じて動作し、ビデオドライバ８に交流化信号ＦＲＰ及びサンプルホールド信号ＳＨＰを供給している。又、タイミングジェネレータ９はＬＣＤ１に対してＨＳＴ，ＨＣＫ，ＶＳＴ，ＶＣＫなどのパネル駆動用パルスと制御信号ＢＬＫＰを供給している。

【００１８】図５は、図４に示した各映像信号の極性を模式的に表わしている。ビデオ信号ｓｉｇは一水平期間（１Ｈ）毎に有効期間とそれ以外のブランキング期間を含んでいる。有効期間内に一行分の画素に対応した薄膜トランジスタのゲートが開き、信号線を介して各画素に映像信号が書き込まれる。映像信号ｓｉｇ１，ｓｉｇ３及びｓｉｇ５は基準電圧に対して１Ｈ毎に極性が反転する。この基準電圧はＬＣＤ１の対向電極に供給される共通電圧ＣＯＭと実質的に等しい。同様に、映像信号ｓｉｇ２，ｓｉｇ４及びｓｉｇ６も１Ｈ毎に極性が反転する。但し、ｓｉｇ１，３，５とｓｉｇ２，４，６は互いに反対極性となっている。例えば、一行目（１ライン目）に着目すると、ｓｉｇ１，３，５はＣＯＭに対して＋Ｖの電圧を有し、ｓｉｇ２，４，６はＣＯＭに対して－Ｖの電圧を有する。

【００１９】図６は、図４に示したＬＣＤ１の具体的な構成を示す回路図である。図示する様に、画素ＰＸＬはｎ行×ｍ行のマトリクス配置になっている。合計でｎ本のゲート線Ｘは図示しないがＶシフトレジスタに接続されている。又、合計でｍ本の信号線ＹはＨＳＷを介して６本の入力線５に接続されており、それぞれｓｉｇ１～ｓｉｇ６がサンプリングされる。各ＨＳＷはＨシフトレ

ジスタ3により開閉制御される。本例では6画素同時駆動方式を採用している為、ＨＳＷの個数はm／6となる。各ＨＳＷには切り離し用のスイッチＣＳＷが内蔵されており、制御信号ＢＬＫＰに応じて各ＨＳＷをオフ状態にし、信号線Ｙと入力線５を互いに切り離す。又、各信号線Ｙの他端側にはＲＳＷを内蔵したリフレッシュ回路４が接続されている。このリフレッシュ回路４はＢＬＫＰに応じて全てのＲＳＷをオン状態とし、全ての信号線Ｙを互いに短絡させる。

【００２０】次に、図7ないし図１０を参照して図６に示したＬＣＤの動作を詳細に説明する。まず図7に示す様に、１ライン目につながる薄膜トランジスタＴｒを全てオンすることにより、１ライン目の画素１－１～１－ｍは全て対応する信号線Ｙに電気的に接続される。この時、各ＨＳＷに内蔵したＣＳＷは全てＨシフトレジスタ３側に投入されている。まず、Ｈシフトレジスタ３の制御によりＨＳＷ１が導通状態となり、ＨＳＷ１につながる６本の信号線Ｙ１～Ｙ６を介して、画素１－１～１－６に一度に映像信号ｓｉｇ１～ｓｉｇ６の信号電位が書き込まれる。この結果、画素１－１，１－２，１－３，１－４，１－５，１－６はそれぞれ＋－＋－＋－の極性となる。次いでＨＳＷ１が開き、画素１－１～１－６に書き込まれた電位はホールドされる。この時、ＨＳＷ１につながる６本の信号線Ｙ１～Ｙ６も対応する画素１－１～１－６と同様な極性の信号電位にホールドされる。

【００２１】次に図８に示す様に、ＨＳＷ２が導通状態となり、信号線Ｙ７～Ｙ１２を介して画素１－７～１－１２に＋－＋－＋－の極性の信号電位が書き込まれる。次いでＨＳＷ２が非導通状態となり、画素１－７～１－１２及びこれらにつながる信号線Ｙ７～Ｙ１２に図示の極性の信号電位がホールドされる。この様にして、６画素毎に画素と信号線に所定の映像信号ｓｉｇ１～ｓｉｇ６が書き込まれホールドされていく。１ライン目の画素１－１～１－ｍの全てに信号電位が書き込まれると、１ライン目の薄膜トランジスタＴｒが全て非導通状態となり、一行分の走査は完了する。

【００２２】この様にして一水平期間の内の有効期間が終了しブランキング期間に入る。この時、図９に示す様にタイミングジェネレータから制御信号ＢＬＫＰが入力し、ＣＳＷを介して全てのＨＳＷがオフ状態に置かれる。同時に、リフレッシュ回路４内の全てのＲＳＷがオン状態となり、全信号線Ｙが互いにショートされる。即ち、＋Ｖにチャージされていた奇数列の信号線と－Ｖにチャージされていた偶数列の信号線が互いに短絡状態となり、全信号線Ｙは±０付近の電位（ＣＯＭ）になる。この時、ＨＳＷは全てオフ状態となっているので、ＬＣＤ外部からの電流の出入りは一切ない。＋Ｖにチャージされている信号線と－Ｖにチャージされている信号線がショートされることによって、信号線は全て同電位（ＣＯＭ付近）にリフレッシュされる。

【００２３】次に図１０に示す様に、２ライン目の走査が始まる。この時には、ビデオドライバから、１ライン目とは逆極性となるｓｉｇ１～ｓｉｇ６が供給される。即ち、ｓｉｇ１，３，５はＣＯＭに対して－Ｖの電位を有し、ｓｉｇ２，４，６はＣＯＭに対して＋Ｖの電位となる。２ライン目に対応した薄膜トランジスタＴｒが導通状態になる。この後、ＨＳＷが順次開閉制御され、ｓｉｇ１～ｓｉｇ６は対応する信号線Ｙを介して対応する画素に書き込まれる。即ち、ｓｉｇ１，３，５がサンプリングされた信号線は電位が０から－Ｖに移行し、ｓｉｇ２，４，６がサンプリングされた信号線は電位が０から＋Ｖに移行する。信号線はあらかじめ全て共通電圧付近にリフレッシュされている為、外部のビデオドライバは各信号線にＶだけチャージあるいはディスチャージすればよい。従って、ビデオドライバ内のバッファで消費される電力は従来と比べ大幅に削減可能である。

【００２４】上述した実施例はドット反転駆動の場合であるが、本発明はこれに限られるものではない。基本的に、ある時間に着目してＬＣＤの共通電圧に対して、正極性にホールドされている画素及び信号線と、負極性にホールドされている画素及び信号線が存在すれば、駆動方法によらず本発明は適用可能である。例えば、列毎交互に反対極性の映像信号をサンプリングするコラム反転駆動にも適用可能である。又、行毎に極性が反転する１Ｈ反転においても、例えば一垂直ブランキング期間にリフレッシュを行なうことができる。一垂直ブランキング期間に、全ゲート線につながる薄膜トランジスタをオン状態におくとともに、全信号線を互いに短絡させることで、所望のリフレッシュを行なうことが可能である。

【００２５】図１１は、アクティブマトリクス表示装置の参考例を示すブロック図である。図６に示した実施例と対応する部分には対応する参照番号を付して理解を容易にしている。この参考例はリフレッシュ機能を備えていない。

【００２６】続いて図１２～図１４を参照して、図１１に示した参考例の動作を簡潔に説明する。まず図１２に示す様に、１ライン目につながる薄膜トランジスタＴｒが全て導通状態となることにより、１ライン目の画素１－１～１－ｍは全て信号線Ｙにつながる。次いで、ＨＳＷ１が閉じることにより、これにつながる６本の信号線Ｙ１～Ｙ６を介して、画素１－１～１－６に一度に信号電位が書き込まれる。次いでＨＳＷ１が開き、画素１－１～１－６に書き込まれた電位はホールドされる。この時、ＨＳＷ１につながる６本の信号線Ｙ１～Ｙ６も、画素と同様に信号電位がホールドされる。即ち、信号線Ｙ１，Ｙ３，Ｙ５は＋Ｖにチャージされ、信号線Ｙ２，Ｙ４，Ｙ６は－Ｖにチャージされる。

【００２７】続いて図１３に示す様に、ＨＳＷ２が導通状態となり、画素１－７～１－１２に信号電位が書き込まれる。この後、ＨＳＷ２が非導通状態となり、画素１

－7～1－12と信号線Y7～Y12に信号電位がホールドされる。Y7，Y9，Y11は＋Vにホールドされ、Y8，Y10，Y12は－Vにホールドされる。以下同様にして、6画素毎に画素と信号線に信号電位が書き込まれホールドされていく。1ライン目の画素1－1～1－mに全て信号電位が書き込まれると、1ライン目の薄膜トランジスタ（画素スイッチ）Trが全てオフ状態となり、1ライン目の走査は完了する。

【0028】この後図14に示す様に、ビデオドライバから1ライン目とは逆極性の映像信号sig1～sig6が供給される。sig1，3，5はCOMに対して負極性の電位となり、sig2，4，6はCOMに対して正極性の電位となる。次いで、2ライン目の薄膜トランジスタTrがオン状態となった後、HSWが順次開閉制御され、sig1～sig6が各信号線を介して画素に書き込まれていく。信号線Y1，Y3，Y5に着目すると、1ライン目では＋Vにホールドされていた電位が2ライン目では－Vに書き換えられる。この時、ビデオドライバ側のバッファは2Vのディスチャージを行わなければならない。又信号線Y2，Y4，Y6に着目すると、1ライン目では－Vにホールドされていた電位が2ライン目では＋Vに書き換えられる。この時、ビデオドライバ側のバッファは2Vのチャージを行なわなければならない。この様に、ビデオドライバ内のバッファは大きな電力を消費する。

【0029】

【発明の効果】以上説明したように、本発明によれば、アクティブマトリクス表示装置はリフレッシュ回路を内蔵しており、映像信号のブランキング期間に信号線を外部から一時的に切り離すとともに、互いに反対極性の映像信号がサンプリングされていた複数の信号線をブランキング期間で内部的に短絡させ、各信号線の電荷を外部から切り離した状態で内部的に中和する。従来のアクティブマトリクス表示装置では、外部と接続した状態で信号線の電位を共通電圧（基準電圧）に対して負側から正側、あるいは正側から負側に充放電していた。これに対し、本発明を用いれば、アクティブマトリクス表示装置内部の電荷のみで信号線電位を共通電圧付近にリフレッシュできる為、外部回路からの充放電を大幅に減らすことができ、ディスプレイシステム全体での消費電力を削減することが可能である。

【図面の簡単な説明】

【図1】本発明に係るアクティブマトリクス表示装置の実施形態を示す回路図である。

【図2】図1に示した実施形態に含まれるリフレッシュ回路の具体的な構成を示す回路図である。

【図3】本発明に係るディスプレイシステムの全体構成を示すブロック図である。

【図4】本発明に係るディスプレイシステムの実施例を示すブロック図である。

【図5】図4に示した実施例の動作説明に供するタイミングチャートである。

【図6】図4に示した実施例に含まれるアクティブマトリクス表示装置の具体的な構成を示す回路図である。

【図7】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図8】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図9】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図10】図6に示したアクティブマトリクス表示装置の動作説明に供する回路図である。

【図11】アクティブマトリクス表示装置の参考例を示す回路図である。

【図12】図11に示した参考例の動作説明に供する回路図である。

【図13】図11に示した参考例の動作説明に供する回路図である。

【図14】図11に示した参考例の動作説明に供する回路図である。

【図15】従来のアクティブマトリクス表示装置の一例を示す回路図である。

【図16】従来のディスプレイシステムの一例を示すブロック図である。

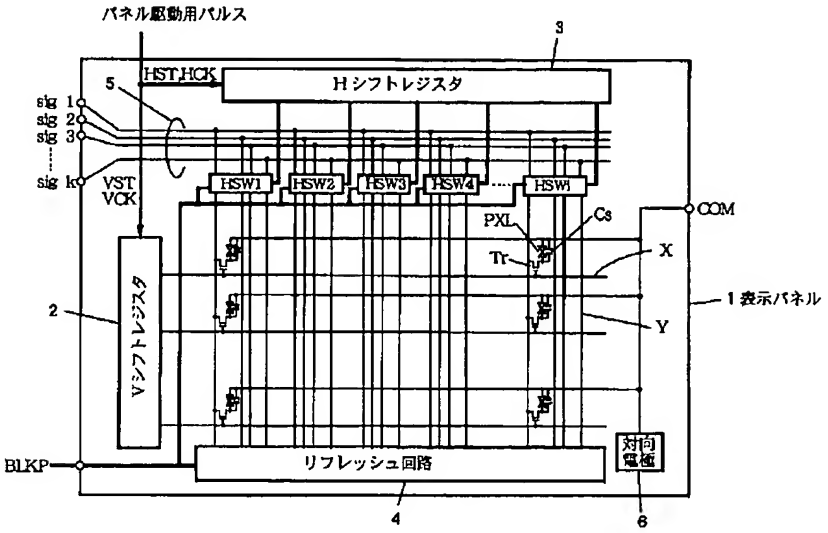
【図17】図16に示した従来のディスプレイシステムの動作説明に供する波形図である。

【図18】図15に示した従来のアクティブマトリクス表示装置の動作説明に供する模式図である。

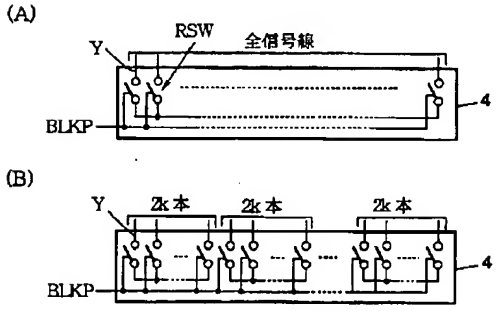
【符号の説明】

1・・・表示パネル、2・・・Vシフトレジスタ、3・・・Hシフトレジスタ、4・・・リフレッシュ回路、5・・・入力線、6・・・対向電極、8・・・ビデオドライバ、9・・・タイミングジェネレータ

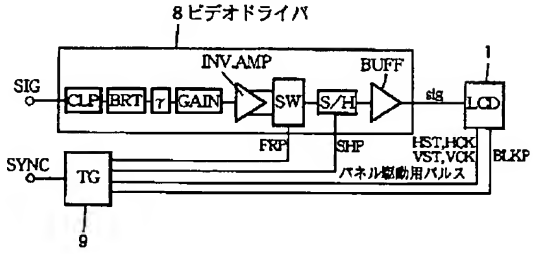
【図1】


パネル駆動用パルス
3
HST,HCK
Hシフトレジスタ
5
sig 1
sig 2
sig 3
sig k
VST
VCK
HSW1
HSW2
HSW3
HSW4
HSWn
COM
PXL
Cs
Tr
X
Y
1 表示パネル
2
Vシフトレジスタ
BLKP
リフレッシュ回路
対向電極
4
6

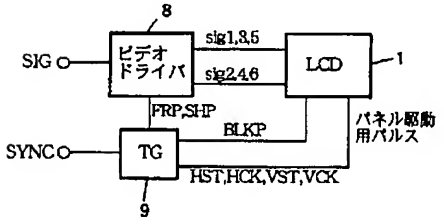
【図2】


(A)
Y
RSW
全信号線
BLKP
4
(B)
Y
2k本
2k本
2k本
BLKP
4

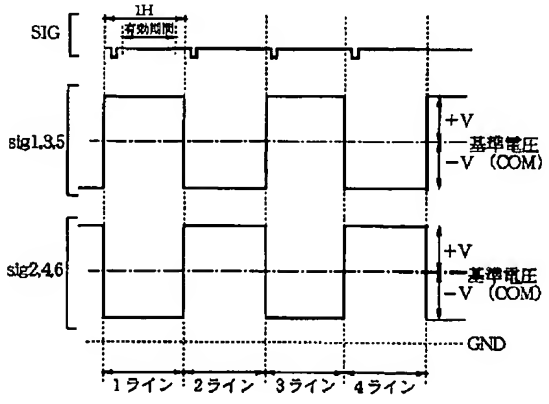
【図3】


8 ビデオドライバ
INV.AMP
BUFF
SIG
CLP
BRT
γ
GAIN
SW
S/H
sig
LCD
1
FRP
SHP
HST,HCK
VST,VCK
BLKP
パネル駆動用パルス
SYNC
TG
9

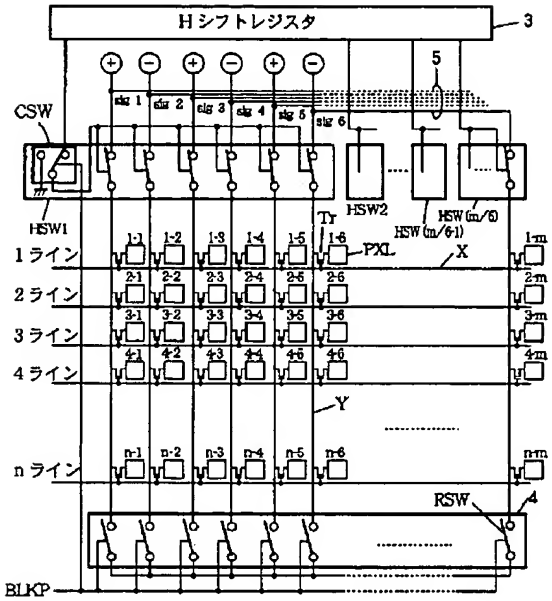
【図4】


8
SIG
ビデオドライバ
sig1,3,5
sig2,4,6
LCD
1
FRP,SHP
BLKP
パネル駆動用パルス
SYNC
TG
HST,HCK,VST,VCK
9

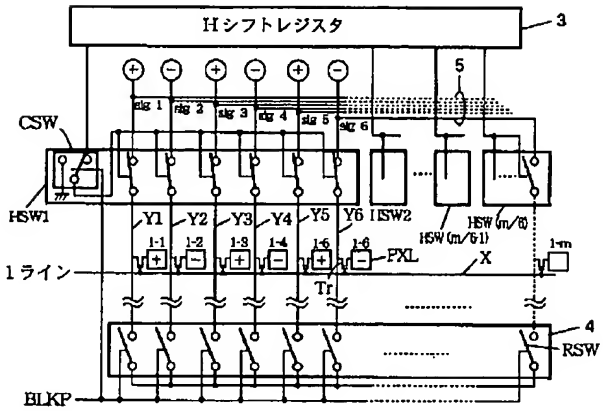
【図5】


SIG
1H
有効期間
sig1,3,5
+V
基準電圧
−V (COM)
sig2,4,6
+V
基準電圧
−V (COM)
GND
1ライン
2ライン
3ライン
4ライン

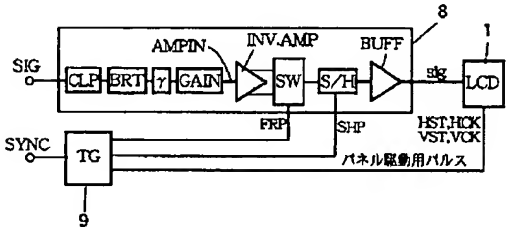
【図6】


Hシフトレジスタ
3
5
CSW
HSW1
HSW2
HSW(m/6)
HSW(m/6-1)
Tr
PXL
X
Y
1ライン
2ライン
3ライン
4ライン
nライン
RSW
4
BLKP

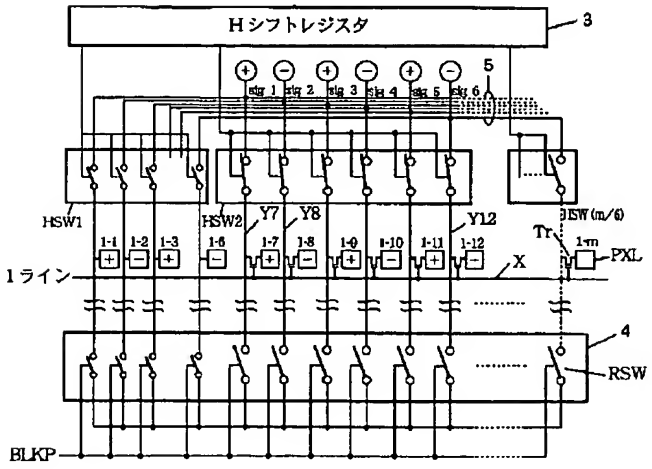
【図7】


Hシフトレジスタ
3
5
CSW
HSW1
Y1
Y2
Y3
Y4
Y5
Y6
HSW2
HSW(m/6)
HSW(m/6-1)
PXL
X
Tr
1ライン
4
RSW
BLKP

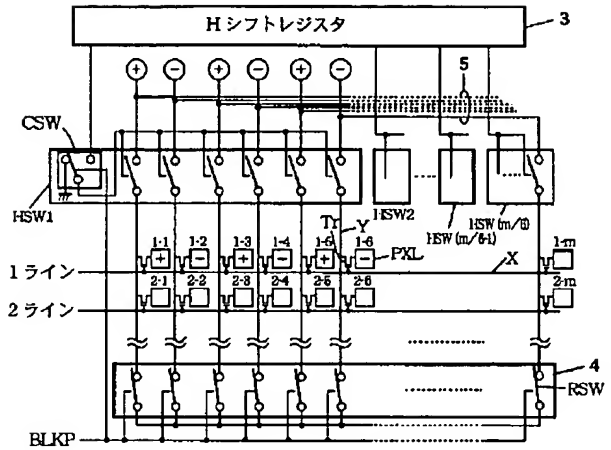
【図16】


8
1
SIG
AMPIN
INV.AMP
BUFF
CLP
BRT
γ
GAIN
SW
S/H
sig
LCD
FRP
SHP
HST,HCK
VST,VCK
SYNC
TG
パネル駆動用パルス
9

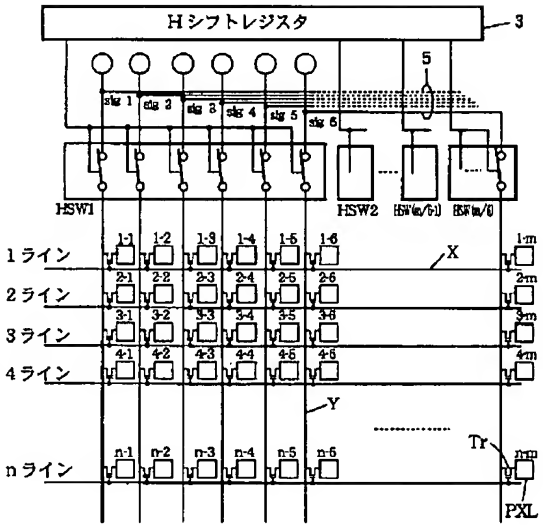
【図8】


Hシフトレジスタ
3
5
HSW1
HSW2
Y7
Y8
Y12
HSW(m/6)
Tr
PXL
X
1ライン
4
RSW
BLKP

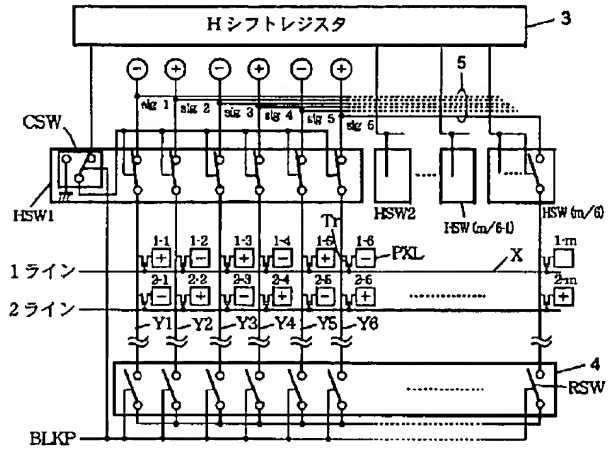
【図9】



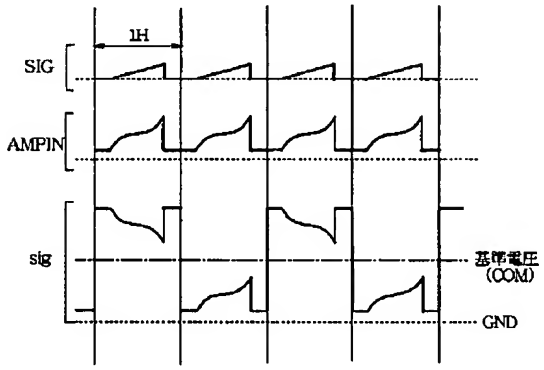
【図11】



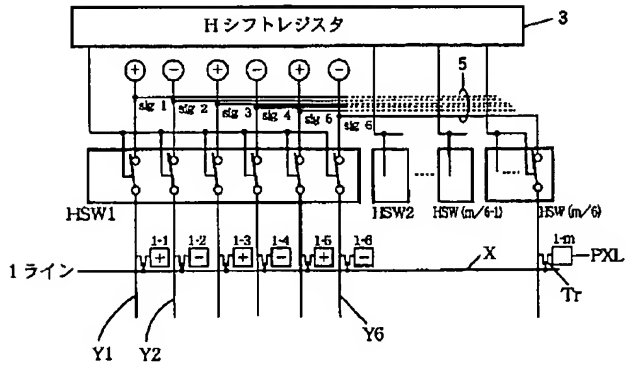
【図10】



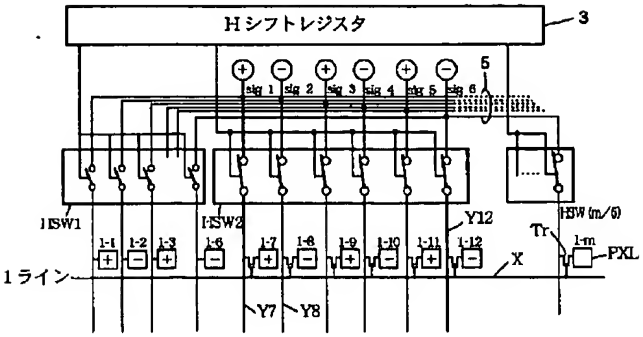
【図17】



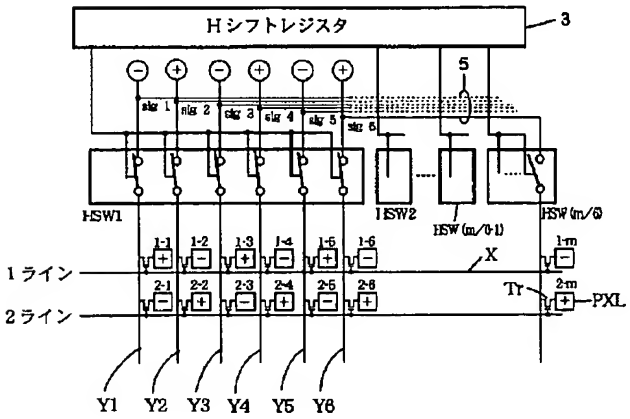
【図12】



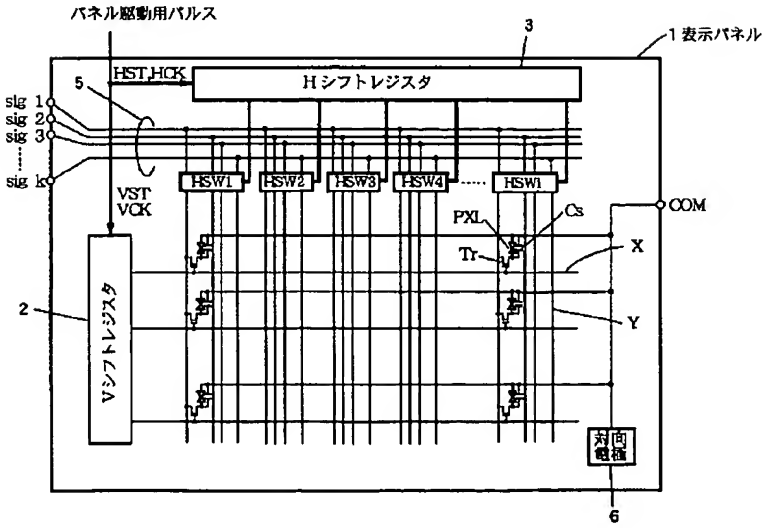
【図13】


Hシフトレジスタ
3
5
sig 1
sig 2
sig 3
sig 4
sig 5
sig 6
HSW1
HSW2
Y12
HSW (m/6)
Tr
1-m
PXL
1-1
1-2
1-3
1-6
1-7
1-8
1-9
1-10
1-11
1-12
X
1ライン
Y7
Y8

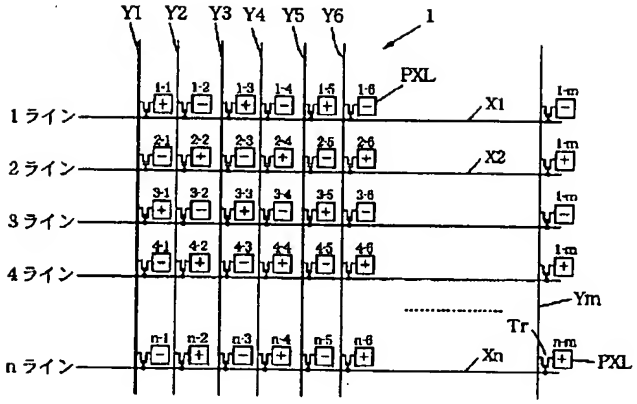
【図14】


Hシフトレジスタ
3
5
sig 1
sig 2
sig 3
sig 4
sig 5
sig 6
HSW1
HSW2
HSW (m/6-1)
HSW (m/6)
1-1
1-2
1-3
1-4
1-5
1-6
1-m
X
1ライン
2-1
2-2
2-3
2-4
2-5
2-6
2-m
Tr
PXL
2ライン
Y1
Y2
Y3
Y4
Y5
Y6

【図15】


パネル駆動用パルス
3
1 表示パネル
HST,HCK
Hシフトレジスタ
5
sig 1
sig 2
sig 3
sig k
VST
VCK
HSW1
HSW2
HSW3
HSW4
HSW1
COM
PXL
Cs
Tr
X
Y
2
Vシフトレジスタ
対向電極
6

【図18】



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(51)Int.Cl. **G09G 3/36**
G02F 1/133

(21)Application number : **09-150347**

(22)Date of filing : **23.05.1997**

(71)Applicant : **SONY CORP**

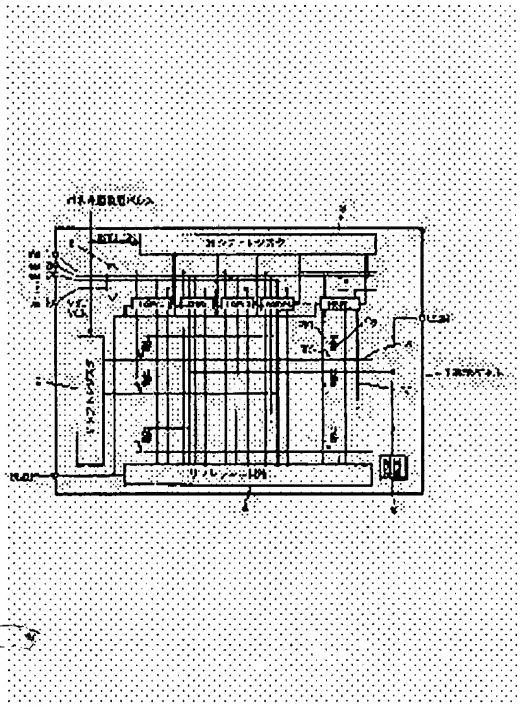
(72)Inventor : **GOTO HISASHI**

(54) ACTIVE MATRIX DISPLAY DEVICE

(57)Abstract:

PROBLEM TO BE SOLVED: To suppress power consumption as the total of a display system in which an active matrix display device is used in a panel.

SOLUTION: This active matrix display device 1 has row shaped gate lines X, column shaped signal lines Y, matrix shaped pixels PXL arranged at intersections of both lines, a V shift register 2 line sequentially scanning respective gate lines X to select pixels PXL equivalent to one row every one horizontal period and an H shift register 3 sampling video signals sig1-sigk supplied from the outside in one horizontal period to respective signal lines Y to write the video signals of sig1-sigk in the selected pixels PXL equivalent to one row. Moreover, the device is provided with a reflesh circuit 4, which temporarily separates the signal lines Y from the outside in blanking periods of the video signals sig1-sigk and short circuits plural signal lines Y in which video signal sig1-sigk whose polarities are opposite each other are sampled internally in the blanking periods to neutralize electric charge of respective signal lines Y internally in a state in which they are separated from the outside.



LEGAL STATUS

[Date of request for examination] 18.03.2003

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[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

CLAIMS

[Claim(s)]
[Claim 1] (41) Color agent 5-amino o-cresol, a 2-amino-4-nitrophenol, A 2-amino-5-nitrophenol, 1-amino-4-methylamino anthraquinone, 3 and 3'-imino diphenol, a hydrochloric acid 2, 4-diamino phenoxyethanol, A hydrochloric acid 2, 4-diaminophenol, hydrochloric-acid toluene -2, 5-diamine, A hydrochloric-acid nitro p phenylenediamine, a hydrochloric-acid p phenylenediamine, A hydrochloric-acid N-phenyl p phenylenediamine, a hydrochloric-acid meta-phenylenediamine, An alt.aminophenol, an acetic-acid N-phenyl p phenylenediamine, 1,4-diaminoanthraquinone, 2, 6-diamino pyridine, 1, 5-dihydroxy naphthalene, Toluene -2, 5-diamine, toluene -3, 4-diamine, a nitro p phenylenediamine, Para-aminophenol, a PARANITORO alt.phenylenediamine, a p phenylenediamine, A PARAME chill aminophenol, a picramic acid, sodium picramate, An N and N'-screw (4-aminophenyl) -2, 5-diamino -1, 4-quinone diimine, 5-(2-hydroxyethylamino)-2-methyl phenol, N-phenyl p phenylenediamine, a meta-aminophenol, a meta-phenylenediamine, sulfuric-acid 5-amino o-cresol, a gate line of behavior A train-like signal line A pixel of a letter of a matrix allotted to each intersection of both A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period A level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from the outside to each signal line, and was chosen within a 1 level period It is the active-matrix indicating equipment equipped with the above, and while separating a signal line temporarily from the exterior at a blanking period of a video signal, it is characterized by having a refresh circuit internally neutralized where it short-circuited internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period and a charge of each signal line is separated from the exterior.
[Claim 2] Said refresh circuit is a active-matrix display according to claim 1 characterized by short-circuiting all signal lines internally while separating all signal lines from the exterior.
[Claim 3] Said refresh circuit is a active-matrix display according to claim 1 characterized by dividing all two or more signal lines into each group, and short-circuiting them by group comrade.
[Claim 4] Said level actuation circuit is a active-matrix display according to claim 1 characterized by sampling a video signal of antipole nature by turns to a signal line arranged in the shape of a train.
[Claim 5] A display system which consists of a video driver which supplies a video signal which polarity reverses to predetermined reference voltage characterized by providing the following, a timing generator which supplies a control signal synchronizing with this video signal, and a display panel which operates according to this control signal and displays an image based on this video signal Said display panel is the gate line of behavior. A train-like signal line A pixel of a letter of a matrix allotted to each intersection of both A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, It has a level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from this external video driver to each signal line, and was chosen within a 1 level period, and displays an image. While separating a signal line from this external video driver temporarily at a blanking period of a video signal according to a control signal supplied from this timing generator A refresh circuit internally neutralized

where it short-circuited internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period and a charge of each signal line is separated from the exterior

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* NOTICES *

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] This invention relates to the active-matrix display (it may be hereafter called a display panel for short) which contained the pixel which constitutes a screen, switching elements, such as a thin film transistor which drives this, and a surrounding actuation circuit. Moreover, it is related with the display system which consists of the video driver which supplies the video signal which reverses polarity to predetermined reference voltage, a timing generator which supplies a control signal synchronizing with a video signal, and a display panel which operates according to a control signal and displays an image based on a video signal.
[0002]
[Description of the Prior Art] With reference to drawing 15 , the conventional active-matrix display is explained briefly. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Pixel PXL consists of the pixel electrode formed in one substrate, a counterelectrode 6 formed in the substrate of another side, and electrooptic material, such as liquid crystal held among both. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. Moreover, the auxiliary capacity Cs is formed corresponding to each pixel PXL. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 and sig2 supplied from an external video driver, ..., sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 constitutes a vertical-drive circuit, answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switches HSW1 and HSW2 which output a sampling pulse one by one and correspond, ..., the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1, ..., the sigk is carried out at the signal line Y which corresponds, respectively.
[0003] In case starting two or more pixel simultaneous sampling actuation is performed, in order to give the amount of delay corresponding to a pixel pitch beforehand to k video signals sig1 - sigk relatively, the sample hold circuit is established in the video driver. While carrying out sample hold of the k video signals serially and giving relatively the amount of delay corresponding to a pixel pitch, by carrying out closing motion control of the group of k signal lines for the level switch HSW simultaneously as an unit, the number of stages contained in the H shift register 3 which drives this level switch can be reduced, and a configuration can be simplified. In addition, a level actuation circuit consists of HSW1 - HSWi,

and an H shift register 3.
[0004] Drawing 16 is the block diagram showing the conventional display system whole configuration. The display system is equipped with the video driver 8, the display panel 1 shown in drawing 15 , and the timing generator (TG) 9. In addition, since a display panel 1 uses liquid crystal (LC) as electrooptic material in many cases, it may be called LCD here. A video driver 8 is changed into the video signal sig which processed the video signal SIG by which an external input is carried out, and was suitable for actuation of LCD1. For example, a video driver 8 performs polarity-reversals processing of a video signal sig in a 1 level period (1H), and outputs the alternating-current-ized video signal sig to LCD1. LCD1 is equipped with the liquid crystal pixel prepared in the gate line of behavior, the train-like signal line, and both intersection as it was shown in drawing 15 . Moreover, the vertical-drive circuit and the level actuation circuit are built in. A vertical-drive circuit scans a gate line sequentially, and chooses a pixel. A level actuation circuit writes the alternating current-ized video signal sig in the pixel chosen as every 1H by carrying out the sequential sampling of the alternating current-ized video signal sig at a signal line. A timing generator 9 operates according to a synchronizing signal SINC, supplies the alternating current-ized signal FRP to a video driver 8, and performs timing control of polarity-reversals processing. Moreover, the sample hold signal SHP is supplied to a video driver 8, and delay processing of a video signal sig is controlled. Namely, a video driver 8 carries out delay processing of two or more video signals sig relatively according to the array pitch of a pixel, and supplies them to LCD1. Further, a timing generator 9 supplies pulses for panel actuation, such as HST, HCK, VST, and VCK, to LCD1, and performs motion control of a vertical-drive circuit and a level actuation circuit.
[0005] The video driver 8 consists of buffers BUFF for a clamping circuit CLP, the bright circuit BRT, the gamma correction circuit gamma, the gain circuit GAIN, inverting circuit INV.AMP, the inversion switch SW, sample hold circuit S/H, and load actuation etc.
[0006] With reference to drawing 17 , actuation of the display system shown in drawing 16 is explained briefly. The pedestal clamp of the video signal SIG inputted from the outside is carried out in a clamping circuit CLP, and the voltage used as criteria is decided. In order to adjust brightness in the bright circuit BRT, bright control of the signal by which the pedestal clamp was carried out is carried out. The signal by which bright control was carried out performs gamma amendment doubled with the property of LCD1 in the gamma correction circuit gamma. A gain adjustment is performed to the signal of which gamma amendment was done in the gain circuit GAIN. The signal AMPIN by which the gain adjustment was carried out is alternating-current-ized by the inversion switch SW. FRP supplied from a timing generator 9 turns on/controls [off] this inversion switch SW. The alternating-current-ized signal passes along sample hold circuit S/H in order to attach the phase contrast suitable for LCD1 which adopts two or more pixel simultaneous actuation. In addition, this sample hold circuit S/H is controlled by SHP supplied from a timing generator 9. The video signal sig by which sample hold was carried out is supplied to LCD1 through Buffer BUFF. It is written in a pixel the k whole dots by HSW1 by which sequential closing motion control of two or more video signals sig1 - the sigk is carried out like - SHWi which were mentioned above at coincidence. In addition, polarity has reversed the video signal sig supplied to LCD1 to predetermined reference voltage to every 1H so that clearly from drawing 17 . This reference voltage is almost equal to the common voltage COM impressed to the counterelectrode 6 shown in drawing 15 .
[0007] Drawing 18 expresses typically the polarity of the video signal sig written in each pixel PXL of LCD1. In this example, six video signals sig1-sig6 are written in coincidence the whole 6 pixels as k= 6. In addition, Pixel PXL constitutes the matrix of a n line m train as a whole. The so-called dot reversal actuation is used for this example. In the 1st line corresponding to the gate line X1, the polar video signals sig1-sig6 of +-+-+- are written in six pixels 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 through signal lines Y1-Y6. In the following line [2nd], the polar video signals sig1-sig6 of -+-+-+ are written in a pixel 2-1, 2-2, 2-3, 2-4, 2-5, and 2-6. Thus, in dot reversal actuation, the video signal sig of antipole nature is mutually written in alternately to the pixel PXL of nxm.
[0008]
[Problem(s) to be Solved by the Invention] As mentioned above, LCD1 needs alternating current

actuation, in order to prevent deterioration of liquid crystal, and it usually needs to reverse a video signal sig to the common voltage COM. this sake COM, for example, common voltage, -- receiving -- a maximum of -- to write the voltage of Vmax in Pixel PXL, it is necessary to make the voltage of 2Vmax (es) change at the maximum for every polarity reversals Therefore, the buffer BUFF equipped with the capacity that the voltage of 2Vmax(es) can be made to change at the maximum, between short time is needed for the external video driver 8. In the display system using the conventional LCD, in order to carry out the charge and discharge of the loads, such as this buffer BUFF and Pixel PXL, and a signal line Y, the current of a large quantity is flowing, and this occupied the great portion of power consumption of a display system.

[0009] In order to solve this problem, the load of the pixel set as the object of charge and discharge or a signal line was mitigated, and voltage impressed to a pixel was reduction-ized. However, in the case of the former, there is a physical limit, and it does not necessarily become sufficient cure. Moreover, in the case of the latter, the side effect of image quality deterioration, such as lowering of contrast, had appeared.

[0010]

[Means for Solving the Problem] The following means were provided in order to solve a technical problem of a Prior art mentioned above. Namely, a active-matrix display (display panel) concerning this invention A pixel of a letter of a matrix allotted to a gate line of behavior, a train-like signal line, and each intersection of both as a fundamental configuration, It has a level actuation circuit which writes a video signal in a vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, and a pixel for a party which sampled a video signal supplied from the outside to each signal line, and was chosen within a 1 level period. As a feature matter, it short-circuits internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period, and where a charge of each signal line is separated from the exterior, this active-matrix indicating equipment is internally neutralized, while it is equipped with a refresh circuit and separates a signal line temporarily from the exterior at a blanking period of a video signal. Preferably, said refresh circuit short-circuits all signal lines internally while separating all signal lines from the exterior. Or said refresh circuit may divide all two or more signal lines into each group, and may be made to short-circuit them by group comrade. In addition, said level actuation circuit samples a video signal of antipole nature by turns to a signal line arranged for example, in the shape of a train.

[0011] This invention includes a display system which used for a display panel a active-matrix indicating equipment mentioned above. This display system consists of a video driver which supplies a video signal which polarity reverses to predetermined reference voltage as a fundamental configuration, a timing generator which supplies a control signal synchronizing with this video signal, and a display panel which operates according to this control signal and displays an image based on this video signal. A pixel of a letter of a matrix matched for a gate line of behavior, a train-like signal line, and each intersection of both with said display panel, A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, It has a level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from this external video driver to each signal line, and was chosen within a 1 level period, and displays an image. As a feature matter, this display panel contains a refresh circuit, and it short-circuits internally two or more signal lines with which a video signal of antipole nature was mutually sampled while separating a signal line from this external video driver temporarily at a blanking period of a video signal according to a control signal supplied from this timing generator in this blanking period, and where a charge of each signal line is separated from the exterior, it neutralizes it internally.

[0012] Usually, display panels, such as LCD, need to carry out the charge and discharge of the twice of voltage written in a pixel in order to reverse a video signal to reference voltage. In this invention, a signal line with which a video signal of straight polarity was sampled inside LCD at a blanking period, and signal line of each other with which a video signal of negative polarity was sampled are short-circuited (short circuit), and a charge is neutralized (cancellation). This reduces a charge which carries

out charge and discharge to a shelf-life, and low-power-ization of a display system is in drawing. When dot reversal actuation is adopted in a active-matrix display panel, specifically, a signal line in a panel is once refreshed on voltage near reference voltage by making all signal lines short-circuit at an image blanking period for every 1 level period. At this time, a signal line in a display panel and an external video driver are refreshed only with a charge inside a panel by dissociating thoroughly. Or in dot reversal actuation, it is also possible to refresh a signal line in a display panel on voltage near reference voltage by making it short-circuit, respectively for every two or more signal lines adjoin an image blanking period for every 1 level period. With the conventional display panel, the charge and discharge of the signal line were carried out to a negative polarity side to reference voltage from a straight polarity or straight polarity side from a negative polarity side by video driver side. According to this invention, since potential of a signal line can be refreshed near reference voltage only with a charge inside a panel, charges and discharges from an external circuit can be reduced substantially, and reduction-izing is possible in power consumption in the whole display system. It is possible to attain low-power-ization, without reduction-izing voltage which reduces loads or is written in a pixel according to this invention.
[0013]
[Embodiment of the Invention] With reference to a drawing, the operation gestalt of this invention is explained to details below. Drawing 1 is the circuit diagram showing the fundamental configuration of the active-matrix display (display panel) concerning this invention. In addition, a corresponding reference number is given to the conventional active-matrix display shown in drawing 15 , and a corresponding portion, and an understanding is made easy. The so-called two or more pixel simultaneous actuation method is used for this operation gestalt. However, this invention is not restricted to this and can be applied also to the line sequential color TV system which writes a video signal in the pixel for the dot sequential system which writes in a video signal for every one pixel, or a party by package. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. Each pixel electrode has met the counterelectrode 6 and electrooptic material, such as liquid crystal, is held among both. The common voltage COM is impressed to the counterelectrode 6 from the exterior. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 supplied from an external video driver - sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. That is, the V shift register 2 constitutes a vertical-drive circuit. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switch HSW1 which outputs a sampling pulse one by one and corresponds - the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1 - the sigk is carried out at the signal line Y which corresponds, respectively. A level actuation circuit consists of an H shift register 3 and HSW.
[0014] This display panel 1 is equipped with the refresh circuit 4 as a feature matter. It short-circuits internally two or more signal lines Y with which the video signal sig1 of antipole nature - sigk were sampled mutually in a blanking period, and where the charge of each signal line Y is separated from the exterior, this refresh circuit 4 is internally neutralized, while it operates according to the control signal BLKP supplied from an external timing generator and separates a signal line Y from an external video driver temporarily at the blanking period of a video signal sig1 - sigk. Specifically, the refresh circuit 4 connects each signal line Y electrically within the main part of the refresh circuit 4 while making an OFF state temporarily the level switch HSW1 - HSWi during a blanking period according to BLKP.

[0015] Drawing 2 shows the concrete example of a configuration of the refresh circuit 4. In the example shown in (A), while separating all the signal lines Y from the exterior, it has the switch RSW for short-circuiting all the signal lines Y internally according to BLKP. On the other hand, in the example of (B), k signal lines Y are divided into each group, for example, and it is short-circuiting each other 2 sets at a time. In addition, this invention is not restricted to this and should just short-circuit the signal line with which the video signal of straight polarity was sampled fundamentally, and the signal line with which the video signal of negative polarity was sampled a same number book every.

[0016] Drawing 3 is the block diagram showing the display system concerning this invention. In addition, in order to make an understanding easy, the corresponding reference number is given to the conventional display system shown in drawing 16 , and the corresponding portion. This display system is equipped with the video driver 8, the timing generator 9, and the display panel (LCD) 1 so that it may illustrate. A video driver 8 supplies the video signal sig inverted to predetermined reference voltage. A timing generator 9 supplies the pulse for panel actuation, and a control signal BLKP synchronizing with a video signal sig. LCD1 operates according to the pulse for panel actuation, or a control signal BLKP, and displays an image based on a video signal sig. The pixel of the letter of a matrix matched with LCD1 for the gate line of behavior, a train-like signal line, and each intersection of both like mentioned above, The vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses the pixel for a party for every 1 level period, It has the level actuation circuit which writes a video signal in the pixel for the party which sampled the video signal sig supplied from the external video driver 8 to each signal line, and was chosen within the 1 level period, and displays an image. In addition, the vertical-drive circuit consists of V shift registers, and the level actuation circuit consists of combination of H shift register and the level switch HSW. As a feature matter, LCD1 builds in the refresh circuit. It short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, this refresh circuit is internally neutralized, while it separates a signal line from the external video driver 8 temporarily at the blanking period of a video signal sig according to the control signal BLKP supplied from a timing generator 9.

[0017] Drawing 4 is the block diagram showing the example of the display system concerning this invention. This example adopted the 6-pixel simultaneous actuation method (k= 6), and has adopted the dot reversal actuation method. A video driver 8 processes a video signal SIG, and supplies six video signals 1-sig 6 to LCD1. sig 1-6 is alternating-current-ized, and phase adjustment is performed. The red video signal is assigned to sig1 and sig2, the green video signal is assigned to sig3 and sig4, and the blue video signal is assigned to sig5 and sig6. A timing generator 9 operates according to a synchronizing signal SYNC, and supplies the alternating current-ized signal FRP and the sample hold signal SHP to the video driver 8. Moreover, the timing generator 9 supplies the pulse for panel actuation and control signals BLKP, such as HST, HCK, VST, and VCK, to LCD1.

[0018] Drawing 5 expresses typically the polarity of each video signal shown in drawing 4 . The video signal sig includes the shelf-life and the other blanking period in every 1 level period (1H). A video signal is written for the gate of the thin film transistor corresponding to the pixel for a party in each pixel through an aperture and a signal line within a shelf-life. Polarity reverses video signals sig1, sig3, and sig5 to every 1H to reference voltage. This reference voltage is substantially [as the common voltage COM supplied to the counterelectrode of LCD1] equal. Similarly, polarity also reverses video signals sig2, sig4, and sig6 to every 1H. However, sig 1, 3, and 5 and sig 2, 4, and 6 serve as antipole nature mutually. For example, when its attention is paid to a party eye (the 1st line), sig 1, 3, and 5 has the voltage of +V to COM, and sig 2, 4, and 6 has the voltage of -V to COM.

[0019] Drawing 6 is the circuit diagram showing the concrete configuration of LCD1 shown in drawing 4 . Pixel PXL is matrix arrangement of n line xm line so that it may illustrate. Although n gate lines X are not illustrated in total, it connects with V shift register. Moreover, m signal lines Y are connected to six input lines 5 through HSW in total, and sig1-sig6 are sampled, respectively. Closing motion control of each HSW is carried out with the H shift register 3. In this example, since the 6-pixel simultaneous actuation method is adopted, the number of HSW becomes m/6. It separates to each HSW, and the

switch CSW of business is built in, each HSW is made into an OFF state according to a control signal BLKP, and a signal line Y and the input line 5 of each other are separated. Moreover, the refresh circuit 4 which built in RSW is connected to the other end side of each signal line Y. This refresh circuit 4 makes all RSW(s) an ON state according to BLKP, and short-circuits all the signal lines Y of each other.

[0020] Next, the actuation of LCD shown in drawing 6 with reference to drawing 7 thru/or drawing 10 is explained to details. As first shown in drawing 7 , all of the pixel 1-1 of the 1st line - 1-m are electrically connected to the corresponding signal line Y by turning on altogether the thin film transistor Tr connected with the 1st line. At this time, each CSWs of all built in HSW are supplied to the H shift register 3 side. First, HSW1 will be in switch-on by control of the H shift register 3, and the signal potential of video signals sig1-sig6 is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with HSW1. Consequently, a pixel 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 become the polarity of +1+1+1, respectively. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. It is held by the same polar signal potential as the pixel 1-1 to 1-6 to which six signal lines Y1-Y6 connected with HSW1 also correspond at this time.

[0021] Next, as shown in drawing 8 , HSW2 will be in switch-on and the polar signal potential of +-+-+- is written in a pixel 1-7 to 1-12 through signal lines Y7-Y12. Subsequently, HSW2 will be in non-switch-on, and the polar signal potential of a graphic display is held by the signal lines Y7-Y12 connected with a pixel 1-7 to 1-12, and these. Thus, the predetermined video signals sig1-sig6 are written in and held by the pixel and the signal line every 6 pixels. If signal potential is written in all of the pixels 1-1 of the 1st line - 1-m, the thin film transistor Tr of the 1st line will be in non-switch-on altogether, and will complete the scan for a party.

[0022] Thus, the shelf-life of the 1 level periods expires, and it enters at a blanking period. At this time, as shown in drawing 9 , a control signal BLKP inputs from a timing generator, and all HSW(s) are put on an OFF state through CSW. Simultaneously, all RSW(s) in the refresh circuit 4 will be in an ON state, and all the signal lines Y short-circuit mutually. That is, the signal line of the odd number train charged by +V and the signal line of the even number train charged by -V will be in a short circuit condition mutually, and Y will become the potential (COM) of the **all signal lines 0 neighborhood. Since all HSW(s) are OFF states at this time, receipts and payments of the current from the LCD outside are absolutely none. + When the signal line charged by V and the signal line charged by -V short-circuit, refresh all signal lines in this potential (near COM).

[0023] Next, as shown in drawing 10 , the scan of the 2nd line starts. At this time, sig1-sig6 used as reversed polarity are supplied in the 1st line from a video driver. That is, sig 1, 3, and 5 has the potential of -V to COM, and sig 2, 4, and 6 serves as potential of +V to COM. The thin film transistor Tr corresponding to the 2nd line will be in switch-on. Then, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel which corresponds through the corresponding signal line Y. Namely, as for the signal line with which sig 1, 3, and 5 was sampled, potential shifts to -V from 0, and, as for the signal line with which sig 2, 4, and 6 was sampled, potential shifts to +V from 0. since the signal line is beforehand refreshed near common voltage altogether -- an external video driver -- each signal line -- V -- charge -- or what is necessary is just to carry out a discharge Therefore, the power consumed with the buffer in a video driver is substantially reducible compared with the former.

[0024] Although the example mentioned above is the case of dot reversal actuation, this invention is not restricted to this. If the pixel and signal line which are held by straight polarity to the common voltage of LCD paying attention to a certain time amount, and the pixel and signal line which are held by negative polarity exist fundamentally, it cannot be based on the actuation method but this invention can be applied. For example, it is applicable also to the column reversal actuation which samples the video signal of antipole nature by turns the whole train. Moreover, also in the 1H reversal which polarity reverses for every line, it can refresh at a 1 vertical blanking period, for example. It is possible to refresh a request in short-circuiting [in / for the thin film transistor connected with all gate lines at a 1 vertical blanking period / an ON state] all signal lines of each other.

[0025] Drawing 11 is the block diagram showing the example of reference of a active-matrix indicating

equipment. A corresponding reference number is given to the example shown in drawing 6 , and a corresponding portion, and an understanding is made easy. This example of reference is not equipped with the refresh function.

[0026] Then, with reference to drawing 12 - drawing 14 , actuation of the example of reference shown in drawing 11 is explained briefly. As first shown in drawing 12 , when the thin film transistor Tr connected with the 1st line will be in switch-on altogether, all of the pixel 1-1 of the 1st line - 1-m are connected with a signal line Y. Subsequently, when HSW1 closes, signal potential is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with this. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. At this time, signal potential is held like [six signal lines Y1-Y6 connected with HSW1] a pixel. That is, signal lines Y1, Y3, and Y5 are charged by +V, and signal lines Y2, Y4, and Y6 are charged by -V.

[0027] Then, as shown in drawing 13 , HSW2 will be in switch-on and signal potential is written in a pixel 1-7 to 1-12. Then, HSW2 will be in non-switch-on, and signal potential is held by a pixel 1-7 to 1-12, and signal lines Y7-Y12. Y7, Y9, and Y11 are held by +V, and Y8, Y10, and Y12 are held by -V. Signal potential is written in and held by the pixel and the signal line every 6 pixels like the following. If signal potential is altogether written in the pixel 1-1 of the 1st line - 1-m, the thin film transistor (pixel switch) Tr of the 1st line will be in an OFF state altogether, and will complete the scan of the 1st line.

[0028] As shown in drawing 14 after this, the video signals sig1-sig6 of reversed polarity are supplied in the 1st line from a video driver. sig 1, 3, and 5 serves as potential of negative polarity to COM, and sig 2, 4, and 6 serves as potential of straight polarity to COM. Subsequently, after the thin film transistor Tr of the 2nd line will be in an ON state, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel through each signal line. If its attention is paid to signal lines Y1, Y3, and Y5, the potential currently held by +V in the 1st line will be rewritten by -V by the 2nd line. At this time, the buffer by the side of a video driver must perform the discharge of 2V. Moreover, if its attention is paid to signal lines Y2, Y4, and Y6, the potential currently held by -V in the 1st line will be rewritten by +V by the 2nd line. At this time, the buffer by the side of a video driver must charge 2V. Thus, the buffer in a video driver consumes big power.

[0029]

[Effect of the Invention] According to this invention, as explained above, it short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, the active-matrix indicating equipment is internally neutralized, while it contains the refresh circuit and separates a signal line temporarily from the exterior at the blanking period of a video signal. With the conventional active-matrix display, the charge and discharge of the potential of a signal line were carried out to the negative side from the positive or positive side from a negative side to common voltage (reference voltage) in the condition of having connected with the exterior. On the other hand, if this invention is used, since signal-line potential can be refreshed near common voltage only with the charge inside a active-matrix display, the charge and discharge from an external circuit can be reduced substantially, and it is possible to reduce the power consumption in the whole display system.

[Translation done.]

* NOTICES *

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2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[A technical field to which invention belongs] This invention relates to a active-matrix display (it may be hereafter called a display panel for short) which contained a pixel which constitutes a screen, switching elements, such as a thin film transistor which drives this, and a surrounding actuation circuit. Moreover, it is related with a display system which consists of a video driver which supplies a video signal which reverses polarity to predetermined reference voltage, a timing generator which supplies a control signal synchronizing with a video signal, and a display panel which operates according to a control signal and displays an image based on a video signal.

[Translation done.]

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3.In the drawings, any words are not translated.

PRIOR ART

[Description of the Prior Art] With reference to drawing 15 , the conventional active-matrix display is explained briefly. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Pixel PXL consists of the pixel electrode formed in one substrate, a counterelectrode 6 formed in the substrate of another side, and electrooptic material, such as liquid crystal held among both. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. Moreover, the auxiliary capacity Cs is formed corresponding to each pixel PXL. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 and sig2 supplied from an external video driver, ..., sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 constitutes a vertical-drive circuit, answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switches HSW1 and HSW2 which output a sampling pulse one by one and correspond, ..., the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1, ..., the sigk is carried out at the signal line Y which corresponds, respectively.
[0003] In case starting two or more pixel simultaneous sampling actuation is performed, in order to give the amount of delay corresponding to a pixel pitch beforehand to k video signals sig1 - sigk relatively, the sample hold circuit is established in the video driver. While carrying out sample hold of the k video signals serially and giving relatively the amount of delay corresponding to a pixel pitch, by carrying out closing motion control of the group of k signal lines for the level switch HSW simultaneously as an unit, the number of stages contained in the H shift register 3 which drives this level switch can be reduced, and a configuration can be simplified. In addition, a level actuation circuit consists of HSW1 - HSWi, and an H shift register 3.
[0004] Drawing 16 is the block diagram showing the conventional display system whole configuration. The display system is equipped with the video driver 8, the display panel 1 shown in drawing 15 , and the timing generator (TG) 9. In addition, since a display panel 1 uses liquid crystal (LC) as electrooptic material in many cases, it may be called LCD here. A video driver 8 is changed into the video signal sig which processed the video signal SIG by which an external input is carried out, and was suitable for actuation of LCD1. For example, a video driver 8 performs polarity-reversals processing of a video signal sig in a 1 level period (1H), and outputs the alternating-current-ized video signal sig to LCD1. LCD1 is equipped with the liquid crystal pixel prepared in the gate line of behavior, the train-like signal line, and both intersection as it was shown in drawing 15 . Moreover, the vertical-drive circuit and the

level actuation circuit are built in. A vertical-drive circuit scans a gate line sequentially, and chooses a pixel. A level actuation circuit writes the alternating current-ized video signal sig in the pixel chosen as every 1H by carrying out the sequential sampling of the alternating current-ized video signal sig at a signal line. A timing generator 9 operates according to a synchronizing signal SINC, supplies the alternating current-ized signal FRP to a video driver 8, and performs timing control of polarity-reversals processing. Moreover, the sample hold signal SHP is supplied to a video driver 8, and delay processing of a video signal sig is controlled. Namely, a video driver 8 carries out delay processing of two or more video signals sig relatively according to the array pitch of a pixel, and supplies them to LCD1. Further, a timing generator 9 supplies pulses for panel actuation, such as HST, HCK, VST, and VCK, to LCD1, and performs motion control of a vertical-drive circuit and a level actuation circuit.

[0005] The video driver 8 consists of buffers BUFF for a clamping circuit CLP, the bright circuit BRT, the gamma correction circuit gamma, the gain circuit GAIN, inverting circuit INV.AMP, the inversion switch SW, sample hold circuit S/H, and load actuation etc.

[0006] With reference to drawing 17 , actuation of the display system shown in drawing 16 is explained briefly. The pedestal clamp of the video signal SIG inputted from the outside is carried out in a clamping circuit CLP, and the voltage used as criteria is decided. In order to adjust brightness in the bright circuit BRT, bright control of the signal by which the pedestal clamp was carried out is carried out. The signal by which bright control was carried out performs gamma amendment doubled with the property of LCD1 in the gamma correction circuit gamma. A gain adjustment is performed to the signal of which gamma amendment was done in the gain circuit GAIN. The signal AMPIN by which the gain adjustment was carried out is alternating-current-ized by the inversion switch SW. FRP supplied from a timing generator 9 turns on/controls [off] this inversion switch SW. The alternating-current-ized signal passes along sample hold circuit S/H in order to attach the phase contrast suitable for LCD1 which adopts two or more pixel simultaneous actuation. In addition, this sample hold circuit S/H is controlled by SHP supplied from a timing generator 9. The video signal sig by which sample hold was carried out is supplied to LCD1 through Buffer BUFF. It is written in a pixel the k whole dots by HSW1 by which sequential closing motion control of two or more video signals sig1 - the sigk is carried out like - SHWi which were mentioned above at coincidence. In addition, polarity has reversed the video signal sig supplied to LCD1 to predetermined reference voltage to every 1H so that clearly from drawing 17 . This reference voltage is almost equal to the common voltage COM impressed to the counterelectrode 6 shown in drawing 15 .

[0007] Drawing 18 expresses typically the polarity of the video signal sig written in each pixel PXL of LCD1. In this example, six video signals sig1-sig6 are written in coincidence the whole 6 pixels as k= 6. In addition, Pixel PXL constitutes the matrix of a n line m train as a whole. The so-called dot reversal actuation is used for this example. In the 1st line corresponding to the gate line X1, the polar video signals sig1-sig6 of +-+-+- are written in six pixels 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 through signal lines Y1-Y6. In the following line [2nd], the polar video signals sig1-sig6 of -+-+-+ are written in a pixel 2-1, 2-2, 2-3, 2-4, 2-5, and 2-6. Thus, in dot reversal actuation, the video signal sig of antipole nature is mutually written in alternately to the pixel PXL of nxm.

[Translation done.]

* NOTICES *

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EFFECT OF THE INVENTION

[Effect of the Invention] According to this invention, as explained above, it short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, the active-matrix indicating equipment is internally neutralized, while it contains the refresh circuit and separates a signal line temporarily from the exterior at the blanking period of a video signal. With the conventional active-matrix display, the charge and discharge of the potential of a signal line were carried out to the negative side from the positive or positive side from a negative side to common voltage (reference voltage) in the condition of having connected with the exterior. On the other hand, if this invention is used, since signal-line potential can be refreshed near common voltage only with the charge inside a active-matrix display, the charge and discharge from an external circuit can be reduced substantially, and it is possible to reduce the power consumption in the whole display system.

[Translation done.]

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] As mentioned above, LCD1 needs alternating current actuation, in order to prevent deterioration of liquid crystal, and it usually needs to reverse a video signal sig to the common voltage COM. this sake COM, for example, common voltage, -- receiving -- a maximum of -- to write the voltage of Vmax in Pixel PXL, it is necessary to make the voltage of 2Vmax (es) change at the maximum for every polarity reversals Therefore, the buffer BUFF equipped with the capacity that the voltage of 2Vmax(es) can be made to change at the maximum, between short time is needed for the external video driver 8. In the display system using the conventional LCD, in order to carry out the charge and discharge of the loads, such as this buffer BUFF and Pixel PXL, and a signal line Y, the current of a large quantity is flowing, and this occupied the great portion of power consumption of a display system.
[0009] In order to solve this problem, the load of the pixel set as the object of charge and discharge or a signal line was mitigated, and voltage impressed to a pixel was reduction-ized. However, in the case of the former, there is a physical limit, and it does not necessarily become sufficient cure. Moreover, in the case of the latter, the side effect of image quality deterioration, such as lowering of contrast, had appeared.

[Translation done.]

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MEANS

[Means for Solving the Problem] The following means were provided in order to solve a technical problem of a Prior art mentioned above. Namely, a active-matrix display (display panel) concerning this invention A pixel of a letter of a matrix allotted to a gate line of behavior, a train-like signal line, and each intersection of both as a fundamental configuration, It has a level actuation circuit which writes a video signal in a vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, and a pixel for a party which sampled a video signal supplied from the outside to each signal line, and was chosen within a 1 level period. As a feature matter, it short-circuits internally two or more signal lines with which a video signal of antipole nature was sampled mutually in this blanking period, and where a charge of each signal line is separated from the exterior, this active-matrix indicating equipment is internally neutralized, while it is equipped with a refresh circuit and separates a signal line temporarily from the exterior at a blanking period of a video signal. Preferably, said refresh circuit short-circuits all signal lines internally while separating all signal lines from the exterior. Or said refresh circuit may divide all two or more signal lines into each group, and may be made to short-circuit them by group comrade. In addition, said level actuation circuit samples a video signal of antipole nature by turns to a signal line arranged for example, in the shape of a train.
[0011] This invention includes a display system which used for a display panel a active-matrix indicating equipment mentioned above. This display system consists of a video driver which supplies a video signal which polarity reverses to predetermined reference voltage as a fundamental configuration, a timing generator which supplies a control signal synchronizing with this video signal, and a display panel which operates according to this control signal and displays an image based on this video signal. A pixel of a letter of a matrix matched for a gate line of behavior, a train-like signal line, and each intersection of both with said display panel, A vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses a pixel for a party for every 1 level period, It has a level actuation circuit which writes a video signal in a pixel for a party which sampled a video signal supplied from this external video driver to each signal line, and was chosen within a 1 level period, and displays an image. As a feature matter, this display panel contains a refresh circuit, and it short-circuits internally two or more signal lines with which a video signal of antipole nature was mutually sampled while separating a signal line from this external video driver temporarily at a blanking period of a video signal according to a control signal supplied from this timing generator in this blanking period, and where a charge of each signal line is separated from the exterior, it neutralizes it internally.
[0012] Usually, display panels, such as LCD, need to carry out the charge and discharge of the twice of voltage written in a pixel in order to reverse a video signal to reference voltage. In this invention, a signal line with which a video signal of straight polarity was sampled inside LCD at a blanking period, and signal line of each other with which a video signal of negative polarity was sampled are short-circuited (short circuit), and a charge is neutralized (cancellation). This reduces a charge which carries out charge and discharge to a shelf-life, and low-power-ization of a display system is in drawing. When dot reversal actuation is adopted in a active-matrix display panel, specifically, a signal line in a panel is

once refreshed on voltage near reference voltage by making all signal lines short-circuit at an image blanking period for every 1 level period. At this time, a signal line in a display panel and an external video driver are refreshed only with a charge inside a panel by dissociating thoroughly. Or in dot reversal actuation, it is also possible to refresh a signal line in a display panel on voltage near reference voltage by making it short-circuit, respectively for every two or more signal lines adjoin an image blanking period for every 1 level period. With the conventional display panel, the charge and discharge of the signal line were carried out to a negative polarity side to reference voltage from a straight polarity or straight polarity side from a negative polarity side by video driver side. According to this invention, since potential of a signal line can be refreshed near reference voltage only with a charge inside a panel, charges and discharges from an external circuit can be reduced substantially, and reduction-izing is possible in power consumption in the whole display system. It is possible to attain low-power-ization, without reduction-izing voltage which reduces loads or is written in a pixel according to this invention.
[0013]
[Embodiment of the Invention] With reference to a drawing, the operation gestalt of this invention is explained to details below. Drawing 1 is the circuit diagram showing the fundamental configuration of the active-matrix display (display panel) concerning this invention. In addition, a corresponding reference number is given to the conventional active-matrix display shown in drawing 15 , and a corresponding portion, and an understanding is made easy. The so-called two or more pixel simultaneous actuation method is used for this operation gestalt. However, this invention is not restricted to this and can be applied also to the line sequential color TV system which writes a video signal in the pixel for the dot sequential system which writes in a video signal for every one pixel, or a party by package. The display panel 1 is equipped with the gate line X of behavior, and the train-like signal line Y, and Pixel PXL is formed in both intersection so that it may illustrate. Switching actuation of each pixel PXL is carried out by the corresponding thin film transistor Tr. The gate electrode of a thin film transistor Tr is connected to the corresponding gate line X, a source electrode is connected to the corresponding signal line Y, and the drain electrode is connected to the corresponding pixel electrode. Each pixel electrode has met the counterelectrode 6 and electrooptic material, such as liquid crystal, is held among both. The common voltage COM is impressed to the counterelectrode 6 from the exterior. The display panel 1 is equipped with k input lines 5, and accepts k video signals sig1 supplied from an external video driver - sigk, respectively. As for each signal line Y, k are connected to the predetermined input line 5 through the level switch HSW as one unit. In addition to the above configuration, the display panel 1 contains the V shift register 2 and the H shift register 3. The V shift register 2 answers pulses for panel actuation supplied from an external timing generator, such as the vertical start pulse VST and the vertical clock pulse VCK, operates, scans one gate line X at a time sequentially, and chooses a pixel for every line. That is, the V shift register 2 constitutes a vertical-drive circuit. Pulses for panel actuation, such as the level start pulse HST to which the H shift register 3 is similarly supplied from a timing generator on the other hand, and the level clock pulse HCK, are answered, it operates, and closing motion control of the level switch HSW1 which outputs a sampling pulse one by one and corresponds - the HSWi is carried out, and k signal lines Y are packed as one unit, and are driven. That is, the simultaneous sampling of k video signals sig1 - the sigk is carried out at the signal line Y which corresponds, respectively. A level actuation circuit consists of an H shift register 3 and HSW.
[0014] This display panel 1 is equipped with the refresh circuit 4 as a feature matter. It short-circuits internally two or more signal lines Y with which the video signal sig1 of antipole nature - sigk were sampled mutually in a blanking period, and where the charge of each signal line Y is separated from the exterior, this refresh circuit 4 is internally neutralized, while it operates according to the control signal BLKP supplied from an external timing generator and separates a signal line Y from an external video driver temporarily at the blanking period of a video signal sig1 - sigk. Specifically, the refresh circuit 4 connects each signal line Y electrically within the main part of the refresh circuit 4 while making an OFF state temporarily the level switch HSW1 - HSWi during a blanking period according to BLKP.
[0015] Drawing 2 shows the concrete example of a configuration of the refresh circuit 4. In the example shown in (A), while separating all the signal lines Y from the exterior, it has the switch RSW for short-

circuiting all the signal lines Y internally according to BLKP. On the other hand, in the example of (B), k signal lines Y are divided into each group, for example, and it is short-circuiting each other 2 sets at a time. In addition, this invention is not restricted to this and should just short-circuit the signal line with which the video signal of straight polarity was sampled fundamentally, and the signal line with which the video signal of negative polarity was sampled a same number book every.

[0016] Drawing 3 is the block diagram showing the display system concerning this invention. In addition, in order to make an understanding easy, the corresponding reference number is given to the conventional display system shown in drawing 16 , and the corresponding portion. This display system is equipped with the video driver 8, the timing generator 9, and the display panel (LCD) 1 so that it may illustrate. A video driver 8 supplies the video signal sig inverted to predetermined reference voltage. A timing generator 9 supplies the pulse for panel actuation, and a control signal BLKP synchronizing with a video signal sig. LCD1 operates according to the pulse for panel actuation, or a control signal BLKP, and displays an image based on a video signal sig. The pixel of the letter of a matrix matched with LCD1 for the gate line of behavior, a train-like signal line, and each intersection of both like mentioned above, The vertical-drive circuit which carries out line sequential scanning of each gate line, and chooses the pixel for a party for every 1 level period, It has the level actuation circuit which writes a video signal in the pixel for the party which sampled the video signal sig supplied from the external video driver 8 to each signal line, and was chosen within the 1 level period, and displays an image. In addition, the vertical-drive circuit consists of V shift registers, and the level actuation circuit consists of combination of H shift register and the level switch HSW. As a feature matter, LCD1 builds in the refresh circuit. It short-circuits internally two or more signal lines with which the video signal of antipole nature was sampled mutually in a blanking period, and where the charge of each signal line is separated from the exterior, this refresh circuit is internally neutralized, while it separates a signal line from the external video driver 8 temporarily at the blanking period of a video signal sig according to the control signal BLKP supplied from a timing generator 9.

[0017] Drawing 4 is the block diagram showing the example of the display system concerning this invention. This example adopted the 6-pixel simultaneous actuation method (k= 6), and has adopted the dot reversal actuation method. A video driver 8 processes a video signal SIG, and supplies six video signals 1-sig 6 to LCD1. sig 1-6 is alternating-current-ized, and phase adjustment is performed. The red video signal is assigned to sig1 and sig2, the green video signal is assigned to sig3 and sig4, and the blue video signal is assigned to sig5 and sig6. A timing generator 9 operates according to a synchronizing signal SYNC, and supplies the alternating current-ized signal FRP and the sample hold signal SHP to the video driver 8. Moreover, the timing generator 9 supplies the pulse for panel actuation and control signals BLKP, such as HST, HCK, VST, and VCK, to LCD1.

[0018] Drawing 5 expresses typically the polarity of each video signal shown in drawing 4 . The video signal sig includes the shelf-life and the other blanking period in every 1 level period (1H). A video signal is written for the gate of the thin film transistor corresponding to the pixel for a party in each pixel through an aperture and a signal line within a shelf-life. Polarity reverses video signals sig1, sig3, and sig5 to every 1H to reference voltage. This reference voltage is substantially [as the common voltage COM supplied to the counterelectrode of LCD1] equal. Similarly, polarity also reverses video signals sig2, sig4, and sig6 to every 1H. However, sig 1, 3, and 5 and sig 2, 4, and 6 serve as antipole nature mutually. For example, when its attention is paid to a party eye (the 1st line), sig 1, 3, and 5 has the voltage of +V to COM, and sig 2, 4, and 6 has the voltage of -V to COM.

[0019] Drawing 6 is the circuit diagram showing the concrete configuration of LCD1 shown in drawing 4 . Pixel PXL is matrix arrangement of n line xm line so that it may illustrate. Although n gate lines X are not illustrated in total, it connects with V shift register. Moreover, m signal lines Y are connected to six input lines 5 through HSW in total, and sig1-sig6 are sampled, respectively. Closing motion control of each HSW is carried out with the H shift register 3. In this example, since the 6-pixel simultaneous actuation method is adopted, the number of HSW becomes m/6. It separates to each HSW, and the switch CSW of business is built in, each HSW is made into an OFF state according to a control signal BLKP, and a signal line Y and the input line 5 of each other are separated. Moreover, the refresh circuit

4 which built in RSW is connected to the other end side of each signal line Y. This refresh circuit 4 makes all RSW(s) an ON state according to BLKP, and short-circuits all the signal lines Y of each other.

[0020] Next, the actuation of LCD shown in drawing 6 with reference to drawing 7 thru/or drawing 10 is explained to details. As first shown in drawing 7 , all of the pixel 1-1 of the 1st line - 1-m are electrically connected to the corresponding signal line Y by turning on altogether the thin film transistor Tr connected with the 1st line. At this time, each CSWs of all built in HSW are supplied to the H shift register 3 side. First, HSW1 will be in switch-on by control of the H shift register 3, and the signal potential of video signals sig1-sig6 is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with HSW1. Consequently, a pixel 1-1, 1-2, 1-3, 1-4, 1-5, and 1-6 become the polarity of +1+1+1, respectively. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. It is held by the same polar signal potential as the pixel 1-1 to 1-6 to which six signal lines Y1-Y6 connected with HSW1 also correspond at this time.
[0021] Next, as shown in drawing 8 , HSW2 will be in switch-on and the polar signal potential of +-+-+- is written in a pixel 1-7 to 1-12 through signal lines Y7-Y12. Subsequently, HSW2 will be in non-switch-on, and the polar signal potential of a graphic display is held by the signal lines Y7-Y12 connected with a pixel 1-7 to 1-12, and these. Thus, the predetermined video signals sig1-sig6 are written in and held by the pixel and the signal line every 6 pixels. If signal potential is written in all of the pixels 1-1 of the 1st line - 1-m, the thin film transistor Tr of the 1st line will be in non-switch-on altogether, and will complete the scan for a party.
[0022] Thus, the shelf-life of the 1 level periods expires, and it enters at a blanking period. At this time, as shown in drawing 9 , a control signal BLKP inputs from a timing generator, and all HSW(s) are put on an OFF state through CSW. Simultaneously, all RSW(s) in the refresh circuit 4 will be in an ON state, and all the signal lines Y short-circuit mutually. That is, the signal line of the odd number train charged by +V and the signal line of the even number train charged by -V will be in a short circuit condition mutually, and Y will become the potential (COM) of the **all signal-lines 0 neighborhood. Since all HSW(s) are OFF states at this time, receipts and payments of the current from the LCD outside are absolutely none. + When the signal line charged by V and the signal line charged by -V short-circuit, refresh all signal lines in this potential (near COM).
[0023] Next, as shown in drawing 10 , the scan of the 2nd line starts. At this time, sig1-sig6 used as reversed polarity are supplied in the 1st line from a video driver. That is, sig 1, 3, and 5 has the potential of -V to COM, and sig 2, 4, and 6 serves as potential of +V to COM. The thin film transistor Tr corresponding to the 2nd line will be in switch-on. Then, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel which corresponds through the corresponding signal line Y. Namely, as for the signal line with which sig 1, 3, and 5 was sampled, potential shifts to -V from 0, and, as for the signal line with which sig 2, 4, and 6 was sampled, potential shifts to +V from 0. since the signal line is beforehand refreshed near common voltage altogether -- an external video driver -- each signal line -- V -- charge -- or what is necessary is just to carry out a discharge Therefore, the power consumed with the buffer in a video driver is substantially reducible compared with the former.
[0024] Although the example mentioned above is the case of dot reversal actuation, this invention is not restricted to this. If the pixel and signal line which are held by straight polarity to the common voltage of LCD paying attention to a certain time amount, and the pixel and signal line which are held by negative polarity exist fundamentally, it cannot be based on the actuation method but this invention can be applied. For example, it is applicable also to the column reversal actuation which samples the video signal of antipole nature by turns the whole train. Moreover, also in the 1H reversal which polarity reverses for every line, it can refresh at a 1 vertical blanking period, for example. It is possible to refresh a request in short-circuiting [in / for the thin film transistor connected with all gate lines at a 1 vertical blanking period / an ON state] all signal lines of each other.
[0025] Drawing 11 is the block diagram showing the example of reference of a active-matrix indicating equipment. A corresponding reference number is given to the example shown in drawing 6 , and a corresponding portion, and an understanding is made easy. This example of reference is not equipped

with the refresh function.
[0026] Then, with reference to drawing 12 - drawing 14 , actuation of the example of reference shown in drawing 11 is explained briefly. As first shown in drawing 12 , when the thin film transistor Tr connected with the 1st line will be in switch-on altogether, all of the pixel 1-1 of the 1st line - 1-m are connected with a signal line Y. Subsequently, when HSW1 closes, signal potential is written in a pixel 1-1 to 1-6 at once through six signal lines Y1-Y6 connected with this. Subsequently, the potential by which HSW1 was written in the aperture and the pixel 1-1 to 1-6 is held. At this time, signal potential is held like [six signal lines Y1-Y6 connected with HSW1] a pixel. That is, signal lines Y1, Y3, and Y5 are charged by +V, and signal lines Y2, Y4, and Y6 are charged by -V.
[0027] Then, as shown in drawing 13 , HSW2 will be in switch-on and signal potential is written in a pixel 1-7 to 1-12. Then, HSW2 will be in non-switch-on, and signal potential is held by a pixel 1-7 to 1-12, and signal lines Y7-Y12. Y7, Y9, and Y11 are held by +V, and Y8, Y10, and Y12 are held by -V. Signal potential is written in and held by the pixel and the signal line every 6 pixels like the following. If signal potential is altogether written in the pixel 1-1 of the 1st line - 1-m, the thin film transistor (pixel switch) Tr of the 1st line will be in an OFF state altogether, and will complete the scan of the 1st line.
[0028] As shown in drawing 14 after this, the video signals sig1-sig6 of reversed polarity are supplied in the 1st line from a video driver. sig 1, 3, and 5 serves as potential of negative polarity to COM, and sig 2, 4, and 6 serves as potential of straight polarity to COM. Subsequently, after the thin film transistor Tr of the 2nd line will be in an ON state, sequential closing motion control of the HSW is carried out, and sig1-sig6 are written in the pixel through each signal line. If its attention is paid to signal lines Y1, Y3, and Y5, the potential currently held by +V in the 1st line will be rewritten by -V by the 2nd line. At this time, the buffer by the side of a video driver must perform the discharge of 2V. Moreover, if its attention is paid to signal lines Y2, Y4, and Y6, the potential currently held by -V in the 1st line will be rewritten by +V by the 2nd line. At this time, the buffer by the side of a video driver must charge 2V. Thus, the buffer in a video driver consumes big power.

[Translation done.]

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DESCRIPTION OF DRAWINGS

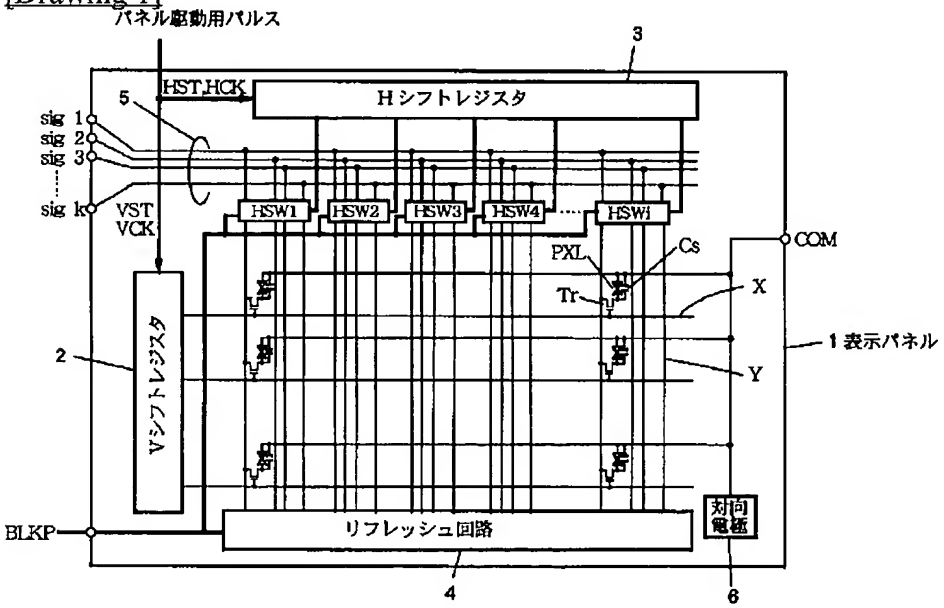
[Brief Description of the Drawings]
[Drawing 1] It is the circuit diagram showing the operation gestalt of the active-matrix display concerning this invention.
[Drawing 2] It is the circuit diagram showing the concrete configuration of the refresh circuit included in the operation gestalt shown in drawing 1 .
[Drawing 3] It is the block diagram showing the whole display system configuration concerning this invention.
[Drawing 4] It is the block diagram showing the example of the display system concerning this invention.
[Drawing 5] It is the timing chart with which explanation of the example shown in drawing 4 of operation is presented.
[Drawing 6] It is the circuit diagram showing the concrete configuration of the active-matrix display contained in the example shown in drawing 4 .
[Drawing 7] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.
[Drawing 8] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.
[Drawing 9] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.
[Drawing 10] It is the circuit diagram with which explanation of the active-matrix display shown in drawing 6 of operation is presented.
[Drawing 11] It is the circuit diagram showing the example of reference of a active-matrix display.
[Drawing 12] It is the circuit diagram with which explanation of the example of reference shown in drawing 11 of operation is presented.
[Drawing 13] It is the circuit diagram with which explanation of the example of reference shown in drawing 11 of operation is presented.
[Drawing 14] It is the circuit diagram with which explanation of the example of reference shown in drawing 11 of operation is presented.
[Drawing 15] It is the circuit diagram showing an example of the conventional active-matrix display.
[Drawing 16] It is the block diagram showing an example of the conventional display system.
[Drawing 17] It is the wave form chart with which explanation of the conventional display system shown in drawing 16 of operation is presented.
[Drawing 18] It is the mimetic diagram with which explanation of the conventional active-matrix display shown in drawing 15 of operation is presented.
[Description of Notations]
1 [... A refresh circuit, 5 / ... An input line, 6 / ... A counterelectrode, 8 / ... A video driver, 9 / ... Timing generator] ... A display panel, 2 ... V shift register, 3 ... H shift register, 4

[Translation done.]

* NOTICES *

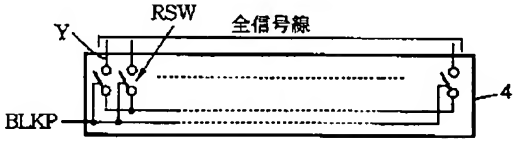
DRAWINGS

[Drawing 1]

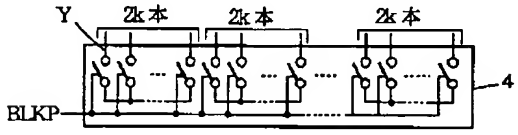


[Drawing 2]

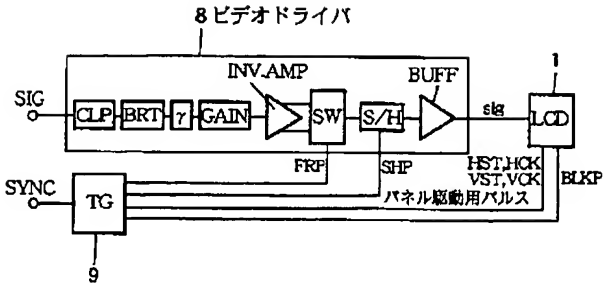
(A)



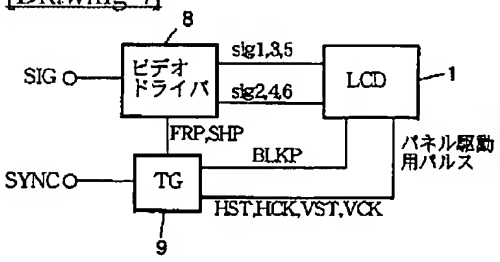
(B)



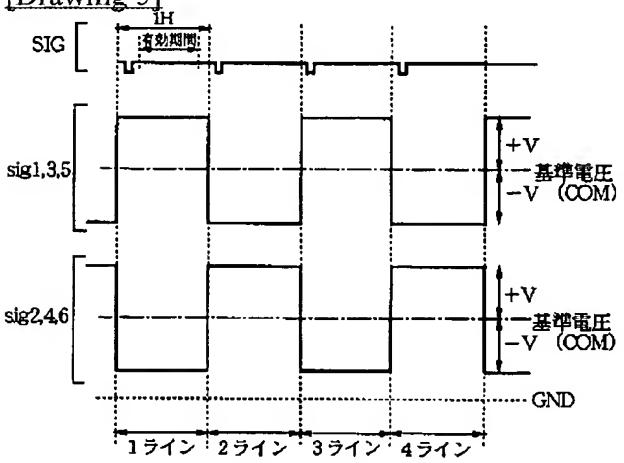
[Drawing 3]



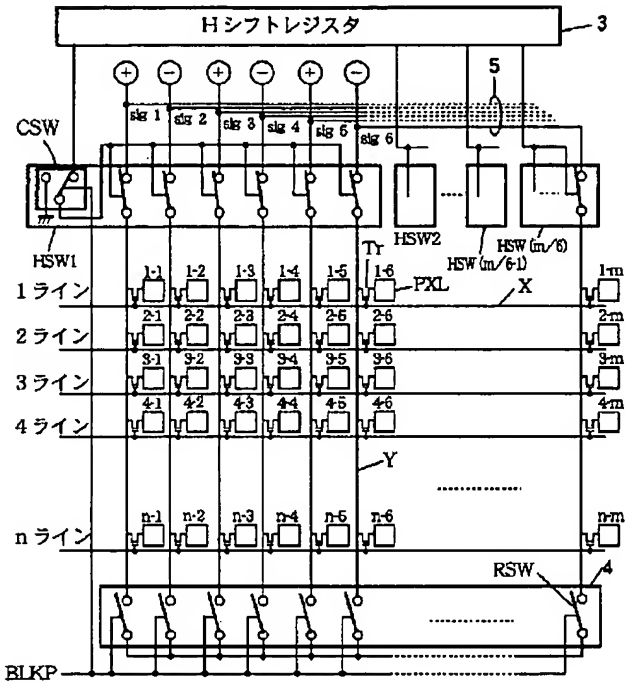
[Drawing 4]



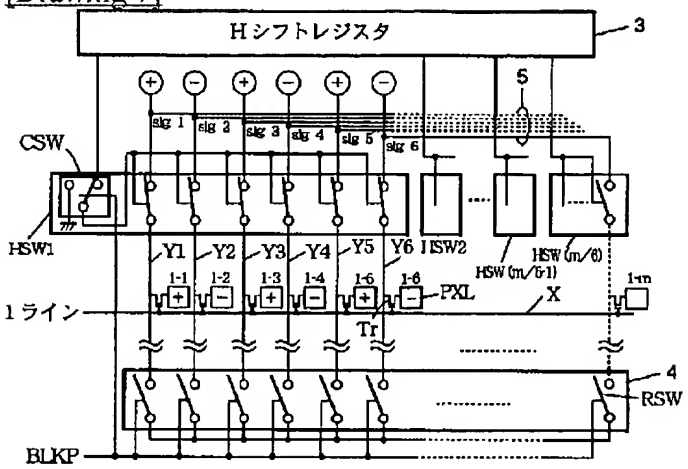
[Drawing 5]



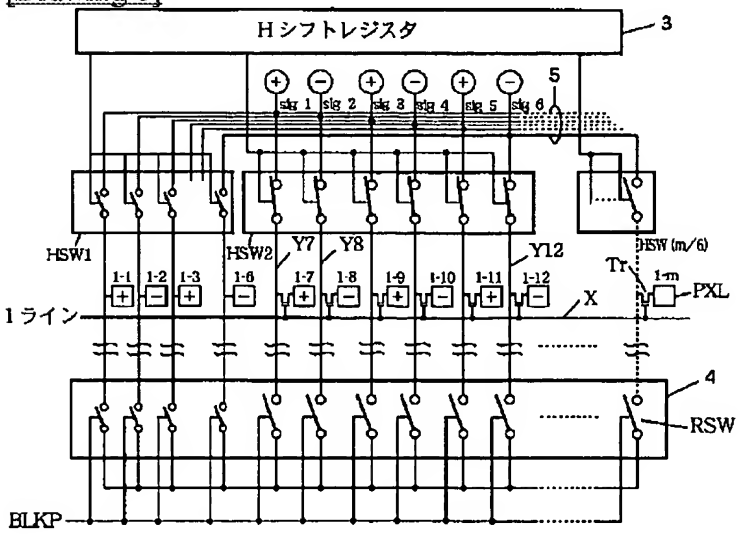
[Drawing 6]



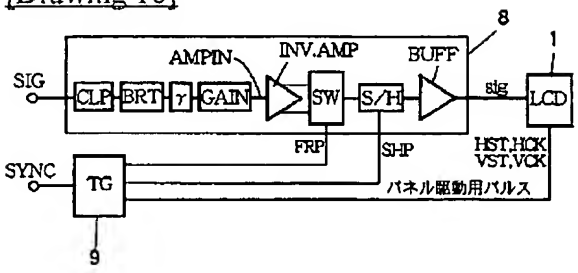
[Drawing 7]



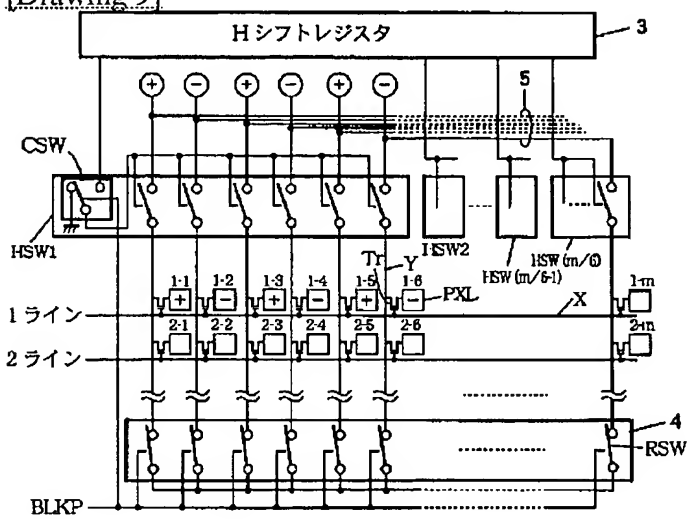
[Drawing 8]



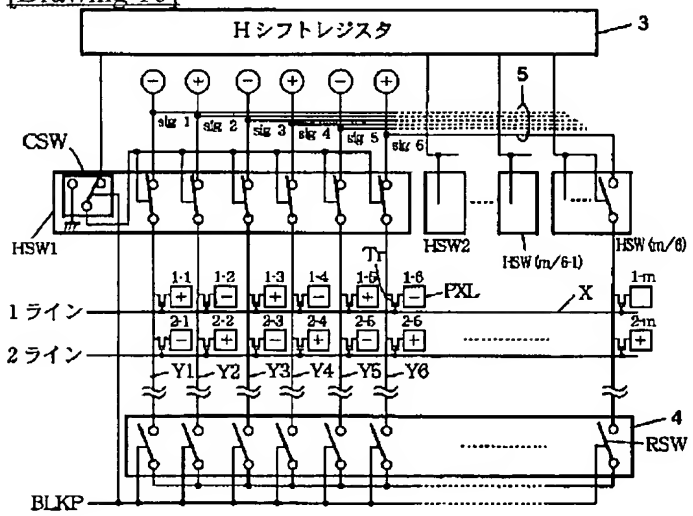
[Drawing 16]



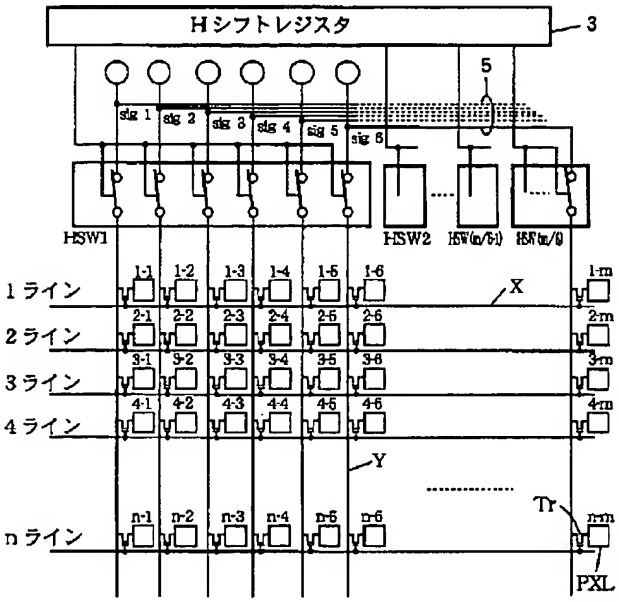
[Drawing 9]



[Drawing 10]



[Drawing 11]



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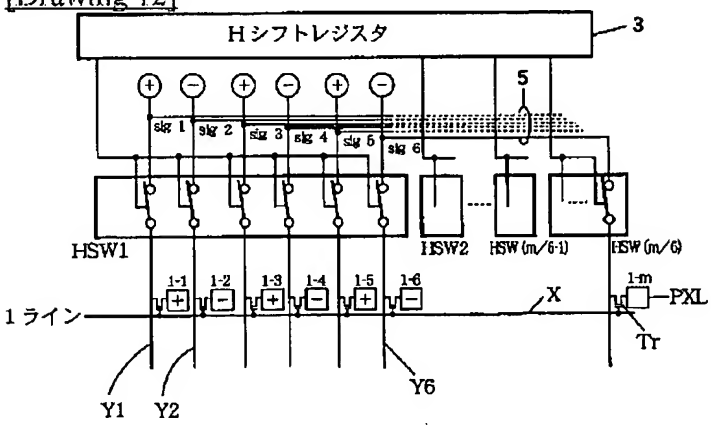
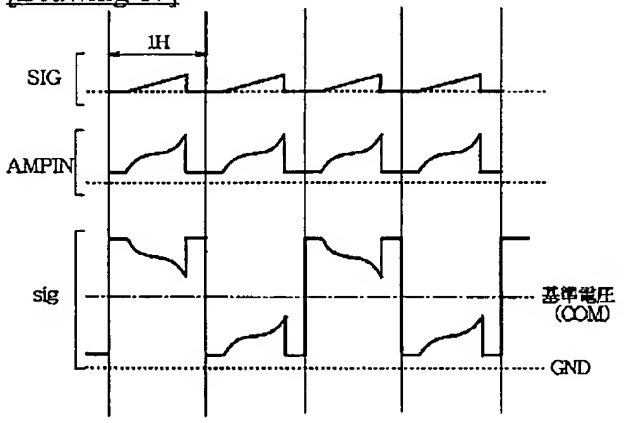
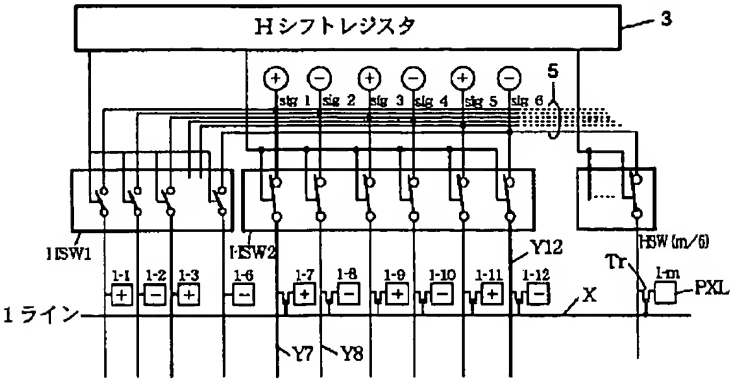


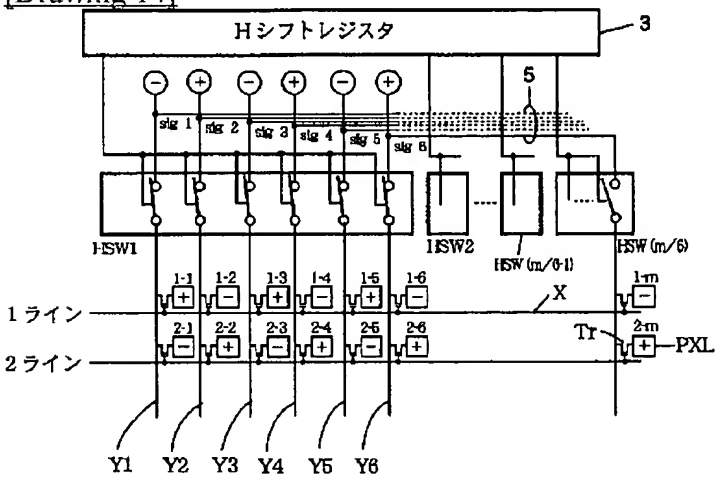
[Drawing 17]



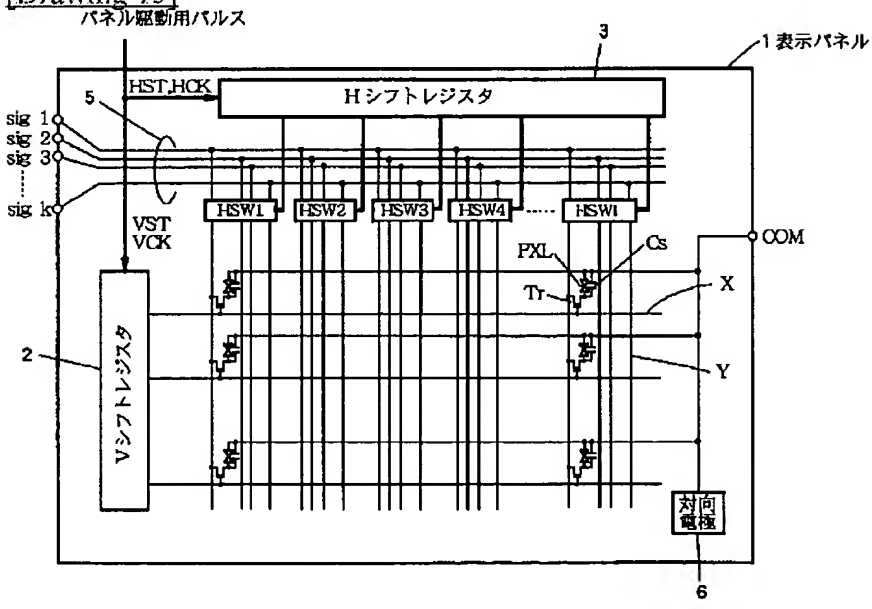
[Drawing 13]



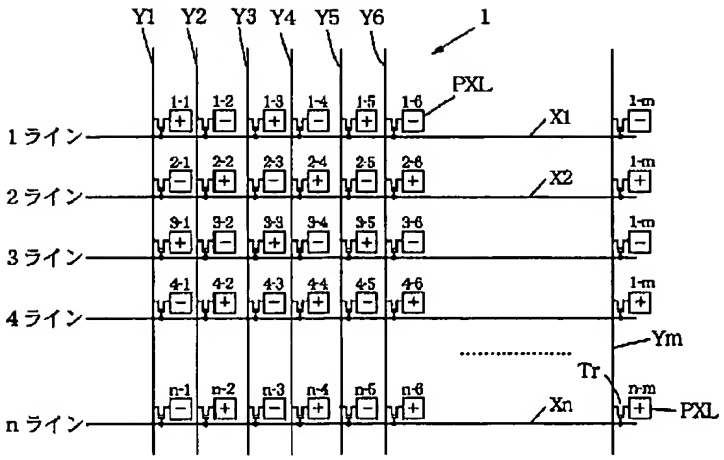
[Drawing 14]



[Drawing 15]



[Drawing 18]



[Translation done.]